15.2 NC161

15.2.1 Technical Data

Module ID	NC161
General Information	
Model Number	7NC161.7
Short Description	2003 encoder module, input frequency 100 kHz, incremental or absolute, 32 bit, encoder supply 5 VDC or 24 VDC, screw-in module
C-UL-US Listed	Yes
B&R ID Code	$10
Module Type	B&R 2003 screw-in module
Slot	AF101 adapter module, CP interface
Power Consumption	0.3 W + $I_{encoder}$ * 5.4 V
Encoder Input	
General Information	Connection using 15 pin D-type socket incremental or SSI absolute encoder
Incremental Encoder Signal Form Evaluation Input Frequency Counter Frequency Phase Shift between Channel A and B Counter Size Inputs Input Level	 Square wave pulses 4-fold Max. 100 kHz Max. 400 kHz 90° ±15° 32 Bit A, A\, B, B\, R, R\ 5 V (differential input)
SSI Absolute Encoder Coding Word Size Baudrate Data Input Level Clock Output Level Max. Signal Delay Clock - Data	 Gray, Binary Max. 31 Bit 100 kBaud 5 V (differential signal) 5 V (differential signal) ≤2.5µs

Module ID	NC161
Additional Inputs +24 VDC	
Reference Enable Switch	Connected using terminal block
Electrical Isolation	Yes
Reference Pulse	Connected using 15 pin D-type socket (pin 10 and 11)
Electrical Isolation	Yes
Encoder Supply	
Output Voltage	+5 VDC / max. 500 mA without external feed
Protection	Short Circuit and Overload Protection
External Supply Voltage	+24 VDC / max. 300 mA
Protection	Short circuit protection
Mechanical Characteristics	
Dimensions	B&R 2003 screw-in module

15.2.2 General Information

The NC161 is an encoder module with symmetrical incremental encoder or absolute encoder evaluation. A 5 V encoder supply is available directly on the module. A 24 V encoder supply must be connected externally to terminals 1 and 2 on the terminal block. The reference enable switch is connected to terminals 3 and 4 .

15.2.3 Operating Modes

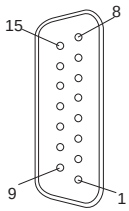
The NC161 is used for single axis positioning with ramps in conjunction with the AO352 analog output module.

15.2.4 Special Functions

- Latches the counter value using the reference enable switch
- Enables use of a comparator output when during incremental encoder operation. The clock output (pins 7 and 8) is used as the comparator output.

15.2.5 Encoder Connection

15 pin D-type socket



Pin	ID	Incremental Encoder	ID	Absolute Encoder	ID	Additional Input	ID	Encoder Supply
1	A	Channel A						
2	A\	A inverted						
3	B	Channel B						
4	B\	B inverted						
5	R	Reference pulse [1]	D	Data input				
6	R\	R inverted [1]	D\	D inverted				
7			C	Clock output				
8			C\	C inverted				
9							ES	Encoder supply [2] +5 VDC / 500 mA
10						Reference pulse +24 VDC [1]		
11						Reference pulse GND [1]		
12							EG	Encoder supply ⊥
13							ES	Encoder supply [3] +24 VDC / 300 mA external voltage from terminal block
14								
15								

[1] Pins 5 and 6 as well as 10 and 11 are linked together using OR logic (hardware). Open pins are considered 0.

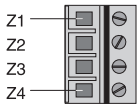
[2] The 5 V encoder supply is not supplied externally. Bit 7 of configuration word 8 must be set in order to activate the 5 V encoder supply.

[3] In order to use an encoder requiring a 24 V power supply, terminals 1 and 2 on the terminal block must be connected to an external 24 V encoder supply.

15.2.6 Terminal Blocks

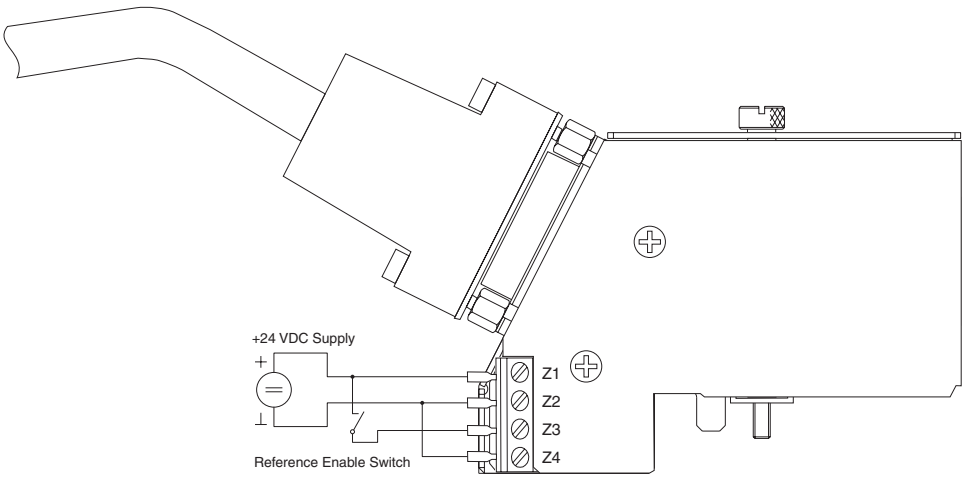
The terminal block is found on the bottom of the module. It is integrated in the housing.

Pin Assignments



Pin	Assignment
1	Feed for external encoder supply max. +24 VDC
2	GND
3	Input reference enable switch +24 VDC
4	Input reference enable switch GND

Connection Example



15.2.7 Variable Declaration for Incremental Encoder Operation

The variable declaration is valid for the following controllers:

- 2003 PCC CPU
- Remote I/O Bus Controller
- CAN Bus Controller

The variable declaration is made in PG2000. The variable declaration is described in Chapter 4, "Module Addressing".

Automation Studio™ Support: See Automation Studio™ Help starting with V 1.40

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Incremental encoder operation with PCC 2003 CPU and remote slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	WORD	Transp. In	0	●		Module status
Data word 1	INT32	Transp. In	2	●		Counter value
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
	INT32	Transp. Out	8		●	Threshold value 1
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
	INT32	Transp. Out	12		●	Threshold value 2
Configuration word 8	WORD	Transp. Out	16		●	Incremental encoder / comparator control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

Incremental Encoder Operation with CAN Slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	INT32	Transp. In	0	●		Counter value
Data word 2	WORD	Transp. In	4	●		Module status
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
	INT32	Transp. Out	8		●	Threshold value 1
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
	INT32	Transp. Out	12		●	Threshold value 2
Configuration word 8	WORD	Transp. Out	16		●	Incremental encoder / comparator control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

B&R 2000 users have to exchange the two counter status words so that the high word is first (Motorola format)!

Access using CAN Identifiers

Access via CAN Identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN Identifiers is described in an example in Chapter 4, "Module Addressing".
The transfer modes are explained in Chapter 5, "CAN Bus Controller Functions".

Data cannot be packed on the NC161. Therefore one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four NC161 modules, the CAN object has the following structure:

Slot	CAN ID [1]	Word 1		Word 2		Word 3		Word 4
1	542	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
2	543	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
3	544	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
4	545	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free

[1] CAN ID = 542 + (nd - 1) x 16 + (ma - 1) x 4 + (sl - 1)
nd ..... Node number of the CAN slave = 1
ma .... Module address of the AF101 = 1
sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see Chapter 5, "CAN Bus Controller Functions".

Description of Data and Configuration Words

Data Word 0 (read)

Data word 0 includes the module status time constant for the counter value.

Bit	Description
12 - 15	x .... Not defined, masked out
11	0.... Counter value not taken 1.... Counter value is taken with the first positive edge on the reference enable switch
10	0.... Counter value not taken 1.... Counter value is taken with the first negative edge on the reference enable switch
9	0.... If bit 8 and bit 9 = 0, then the load is in the valid range or the supply is not switched on 1.... 5 V encoder supply overload or short-circuit
8	0.... If bit 8 and bit 9 = 0, then the load is in the valid range or the supply is not switched on 1.... 5 V encoder supply is not loaded
7	0.... Referencing is taking place 1.... Counter is referenced (resetting takes place when the reference command is received)
6	Changes state each time referencing takes place
5	x .... Not defined, masked out
4	Output status of the comparator
2 - 3	x .... Not defined, masked out
1	Level of the reference enable switch
0	1) Bit 0 in configuration word 14 = 0 Level of the reference pulse 2) Bit 0 in configuration word 14 = 1 Level of the combination of reference pulse and reference enable switch Normal and inverted reference pulses are differentiated. Switching takes place using bit 2 in configuration word 14 (see following explanation).

Normal Reference Pulse:

Please refer to path/status and timing diagrams in the section, "Incremental Encoder Operation".

Bit 0 in Data Word 0 is always 1 when the level of the reference enable switch is 0.
Bit 0 only takes the level of the reference pulse when the level of the reference enable switch is 1.

Bit 0 = Reference pulse or (not reference enable switch)

Reference Pulse	Reference Enable Switch	Bit 0 in Data Word 0
0	0	1
1	0	1
0	1	0
1	1	1

Inverted Reference Pulse:

Bit 0 in data word 0 is always 1 when the level of the reference enable switch is 0.
Bit 0 only takes the level of the inverted reference pulse when the state of the reference enable switch is 1.

Bit 0 = (not reference pulse) or (not reference enable switch)

Reference Pulse	Reference Enable Switch	Bit 0 in Data Word 0
0	0	1
1	0	1
0	1	1
1	1	0

Data Word 1 (read)

Counter Value MSW

Data Word 2 (read)

Counter Value LSW

Configuration Words 4+5 (read)

After setting bit 11 in configuration word 8, the configuration words receive the latched counter value with the first positive edge of the reference enable switch. The value is also valid if bit 11 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in the section, "Incremental Encoder Operation".

Configuration Words 4+5 (write)

Threshold value 1 (32 Bit)

Threshold value 1 must always be ≤ threshold value 2 .
Threshold values are internally arranged in increasing order **including sign**.

Configuration Words 6+7 (read)

After setting bit 10 in configuration word 8, the configuration words receive the latched counter value with the first negative edge of the reference enable switch. The value is also valid if bit 10 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in the section, "Incremental Encoder Operation".

Configuration Words 6+7 (write)

Threshold value 2 (32 Bit)

Configuration Word 8 (write)

Incremental encoders and comparators are configured using configuration word 8.
During incremental encoder operation the clock output (pins 7 and 8) is used as the comparator output.

Bit	Description
12 - 15	0
11	0 ....Counter value not taken 1 ....Counter value is taken with the first positive edge on the reference enable switch (see configuration words 4 and 5) [1]
10	0 ....Counter value not taken 1 ....Counter value is taken with the first negative edge on the reference enable switch (see configuration words 6 and 7) [1]
8 - 9	0
7	0 ....5 V encoder supply off (default) 1 ....5 V encoder supply on
5 - 6	0
4	0 ....No effect on counter 1 Clear counter (reference) With the positive edge on bit 4, the counter is cleared depending on the control signal in configuration word 14 (write). Before further referencing, bit 4 must be reset and set again.
3	0 ....Comparator off The comparator output is set to the level given in bit 0. 1 ....Comparator on
2	0 ....Unconditional comparator output The comparator output is set to the level given in bit 0, if threshold value 1 < counter ≤ threshold value 2 1 ....Conditional comparator output The comparator output can be controlled in two ways: a) Using the reference enable switch, if bit 15 is reset in configuration word 14. Reference enable switch = 1 The comparator output is handled as with "Unconditional comparator output". Reference enable switch = 0 The comparator output is set to the inverted level of bit 0. b) In TPU operation using the TPU-IN line. The line is handled using LTX functions (e.g. with LTXdo0()). TPU operation is defined by setting bit 15 in configuration word 14. TPU-IN line = 1 The comparator output is handled as with "Unconditional comparator output". TPU-IN line = 0 The comparator output is set to the inverted level of bit 0.
1	0
0	Level of the comparator output

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0			0	0		0	0			0		

[1] The counter value is only taken once. Bit 10 and bit 11 must be reset for the value to be taken again. Bit 10 and bit 11 can be set again in configuration word 8 after the corresponding bit in the module status bit has gone to 0.

Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 0.

Configuration Word 14 (read)

The High Byte of configuration word 14 defines the module code.

Bit	Description
8 - 15	Module code = $10
0 - 7	x .... Not defined, masked out

0	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x
15							8	7							0

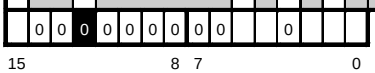
Configuration Word 14 (write)

The module is configured using configuration word 14.

With the standard setting, the encoder module is operated as 32 Bit up/down counter with 4-fold evaluation.

Please refer to path/status and timing diagrams in the section, "Incremental Encoder Operation".

Bit	Description
15	0.... TPU operation switched off 1.... TPU operation switched on To be able to use TPU operation, the module must be operated on the CP Interface. Channels A and B are switched through to the TPU (can be operated using LTX functions e.g. with LTXcab2()). Using the TPU-IN line, the signal source for the TPU-OUT line is selected. Both lines are operated using LTX functions (TPU-IN line e.g. with LTXdo0(), TPU-OUT line e.g. with LTXdi1()). A differentiation must be made as to if the comparator is switched on or off. a) Comparator is switched off (bit 3 in configuration word 8 = 0) TPU-IN = 0... TPU-OUT = reference pulse TPU-IN = 1 TPU-OUT = reference pulse & reference enable switch (binary AND logic) b) Comparator is switched on (bit 2 and bit 3 in configuration word 8 = 1, also compared to status of bit 2 in configuration word 8) TPU-IN = 0... TPU-OUT = inverted level of bit 0 in configuration word 8 TPU-IN = 1... TPU-OUT = Level of bit 0 in configuration word 8, if threshold value 1 < counter ≤ threshold value 2
13 - 14	0
12	0.... Incremental encoder operation 1.... Absolute encoder operation
6 - 11	0
5	0.... No effect on count direction 1.... Reversed count direction
4	0.... Incremental encoder without comparator 1.... Incremental encoder with comparator
3	0
2	0.... No effect on reference pulse 1.... Reference pulse is inverted. This setting is used for encoders with a high pulse.
1	0.... Set counter immediately to 0. In data word 0 (module status), bit 7 is immediately set to 1. 1.... Counter remains functioning. In data word 0 (module status), bit 7 is immediately set to 0 (conditional referencing). Depending on bit 0 in configuration word 14, bit 7 in data word 0 is set to 1 and cleared again with a positive edge on bit 4 in configuration word 8.
0	0.... Ignore reference enable switch (referencing with reference pulse) Refers to bit 4 in configuration word 8. 1.... Activate reference enable switch (referencing with reference pulse and reference enable switch)



15.2.8 Variable Declaration for Absolute Encoder Operation

The variable declaration is valid for the following controllers:

- 2003 PCC CPU
- Remote I/O Bus Controller
- CAN Bus Controller

The variable declaration is made in PG2000. The variable declaration is described in Chapter 4, "Module Addressing".

Automation Studio™ Support: See Automation Studio™ Help starting with V 1.40

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Absolute encoder operation with PCC 2003 CPU and remote slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	WORD	Transp. In	0	●		Module status
Data word 1	INT32	Transp. In	2	●		Counter value
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
Configuration word 8	WORD	Transp. Out	16		●	Absolute encoder control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

Absolute encoder operation with CAN slaves

Data access takes place using data and configuration words. The following table provides an overview of which data and configuration words are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data word 0	INT32	Transp. In	0	●		Counter value
Data word 2	WORD	Transp. In	4	●		Module status
Configuration word 4	INT32	Transp. In	8	●		Counter value at positive edge of the reference enable switch
Configuration word 6	INT32	Transp. In	12	●		Counter value at negative edge of the reference enable switch
Configuration word 8	WORD	Transp. Out	16		●	Absolute encoder control
Configuration word 12	WORD	Transp. In	24	●		Module status
Configuration word 14	WORD	Transp. In	28	●		Module type
	WORD	Transp. Out	28		●	Module configuration

Access using CAN Identifiers

Access via CAN Identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN Identifiers is described in an example in Chapter 4, "Module Addressing".
The transfer modes are explained in Chapter 5, "CAN Bus Controller Functions".

Data cannot be packed on the NC161. Therefore one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four NC161 modules, the CAN object has the following structure:

Slot	CAN ID [1]	Word 1		Word 2		Word 3		Word 4
1	542	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
2	543	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
3	544	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free
4	545	Count. LL	Count. ML	Count. MH	Count. HH	Status L	Status H	Free

[1] CAN ID = 542 + (nd - 1) x 16 + (ma - 1) x 4 + (sl - 1)
nd ..... Node number of the CAN slave = 1
ma .... Module address of the AF101 = 1
sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

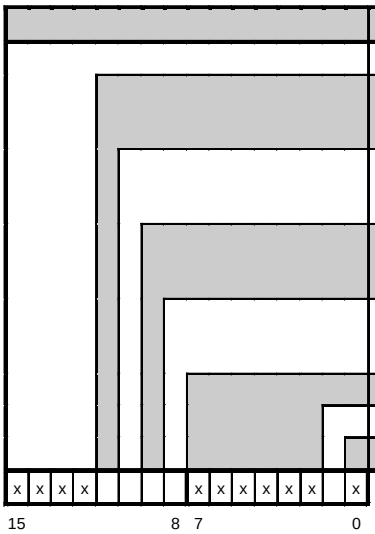
B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see Chapter 5, "CAN Bus Controller Functions".

Description of Data and Configuration Words

Data Word 0 (read)

Data word 0 includes the module status time constant for the counter value.



Bit	Description
12 - 15	x .... Not defined, masked out
11	0 .... Counter value not taken 1 .... Counter value is taken with the first positive edge on the reference enable switch
10	0 .... Counter value not taken 1 .... Counter value is taken with the first negative edge on the reference enable switch
9	0 .... If bit 8 and bit 9 = 0, then the load is in the valid range or the supply is not switched on 1 .... 5 V encoder supply overload or short-circuit
8	0 .... If bit 8 and bit 9 = 0, then the load is in the valid range or the supply is not switched on 1 .... 5 V encoder supply is not loaded
2 - 7	x .... Not defined, masked out
1	Level of the reference enable switch
0	x .... Not defined, masked out

Data Word 1 (read)

Counter Value MSW

Data Word 2 (read)

Counter Value LSW

Configuration Words 4+5 (read)

After setting bit 11 in configuration word 8, the configuration words receive the latched counter value with the first positive edge of the reference enable switch. The value is also valid if bit 11 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in the section, "Incremental Encoder Operation".

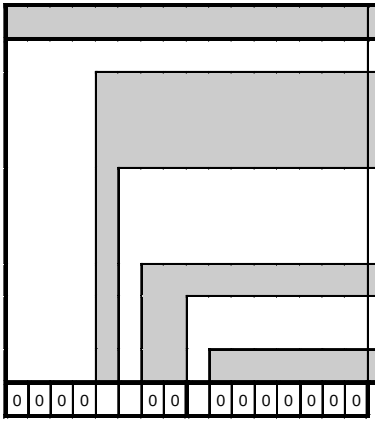
Configuration Words 6+7 (read)

After setting bit 10 in configuration word 8, the configuration words receive the latched counter value with the first negative edge of the reference enable switch. The value is also valid if bit 10 is set in data word 0. Please refer to the timing diagram "Latching the Counter Value" in the section, "Incremental Encoder Operation".

Configuration Word 8 (write)

The absolute encoder is configured using configuration word 8.

Bit	Description
12 - 15	0
11	0.... Counter value not taken 1.... Counter value is taken with the first positive edge on the reference enable switch (see configuration words 4 and 5) [1]
10	0.... Counter value not taken 1.... Counter value is taken with the first negative edge on the reference enable switch (see configuration words 6 and 7) [1]
8 - 9	0
7	0.... 5 V encoder supply off (default) 1.... 5 V encoder supply on
0 - 6	0



[1] The counter value is only taken once. Bit 10 and bit 11 must be reset for the value to be taken again. Bit 10 and bit 11 can be set again in configuration word 8 after the corresponding bit in the module status bit has gone to 0.

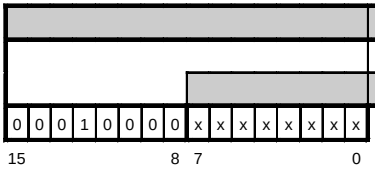
Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 0.

Configuration Word 14 (read)

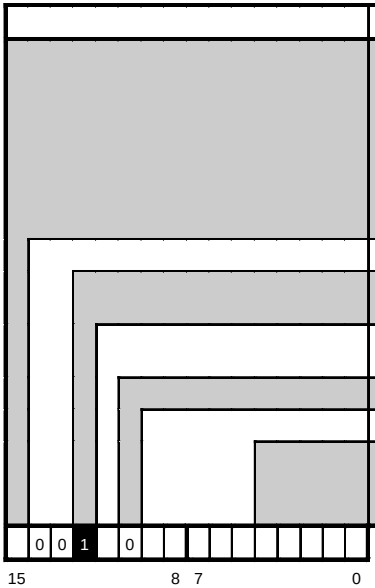
The High Byte of configuration word 14 defines the module code.

Bit	Description
8 - 15	Module code = $10
0 - 7	x.... Not defined, masked out



Configuration Word 14 (write)

The module is configured using configuration word 14.



Bit	Description
15	0.... TPU operation switched off 1.... TPU operation switched on To be able to use TPU operation, the module must be operated on the CP Interface. The TPU-OUT line is used for status information. The line is handled using LTX functions (e.g. with LTXdi1()). TPU-OUT = 0... Position measurement active TPU-OUT = 1... New count available
13 - 14	0
12	0.... Incremental encoder operation 1.... Absolute encoder operation
11	0.... Binary coded SSI encoder signal (SSI encoder) 1.... Gray coded SSI encoder signal
10	0
5 - 9	Number of preceding zeros before the MSB of the encoder value
0 - 4	Number of valid bits in the encoder value As standard, bits 0 - 9 = 0. With this setting, the first 32 bits of the SSI encoder data flow are output.

Please refer to the example in section "Absolute Encoder Information".

15.2.9 Incremental Encoder Operation

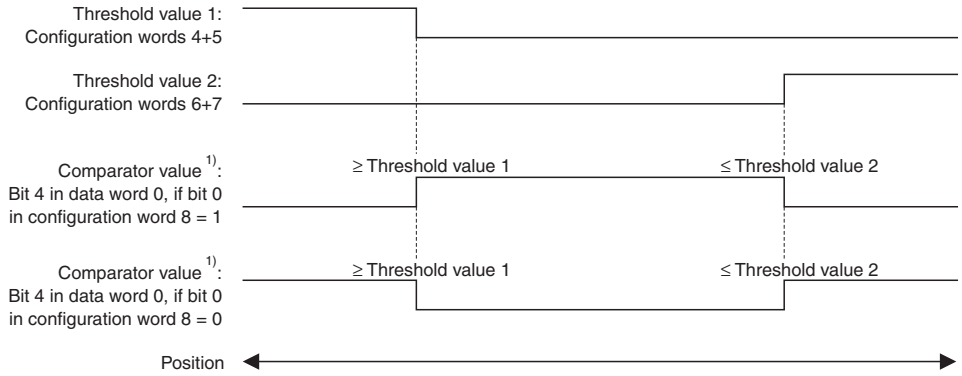
The following path/status and timing diagrams illustrate the functional behavior of the NC161 in incremental encoder operation with various configurations.

Comparator - Unconditional

The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration words 4+5	Threshold value 1	Define threshold value 1 for comparator, threshold value 1 ≤ threshold value 2
Configuration words 6+7	Threshold value 2	Define threshold value 2 for counter
Configuration word 8	Bit 0 = 0 or 1	Level of the comparator output
Configuration word 8	Bit 2 = 0	Unconditional comparator output
Configuration word 8	Bit 3 = 1	Switch comparator on
Configuration word 14	Bit 4 = 1	Incremental encoder operation with comparator
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Path/Status Diagram



1) The comparator shows jitter of 0 - ca. 1 ms

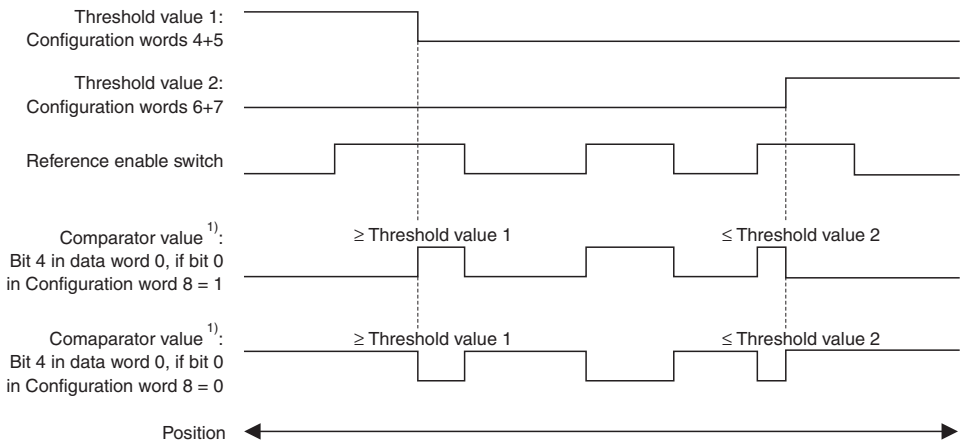
The clock output (pins 7 and 8) correspond to the comparator status of bit 4 in data word 0.

Comparator - Conditional

The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration words 4+5	Threshold value 1	Define threshold value 1 for comparator, threshold value 1 ≤ threshold value 2
Configuration words 6+7	Threshold value 2	Define threshold value 2 for counter
Configuration word 8	Bit 0 = 0 or 1	Level of the comparator output
Configuration word 8	Bit 2 = 1	Conditional comparator output
Configuration word 8	Bit 3 = 1	Switch comparator on
Configuration word 14	Bit 4 = 1	Incremental encoder operation with comparator
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Path/Status Diagram



1) The comparator shows jitter of 0 - ca. 1 ms

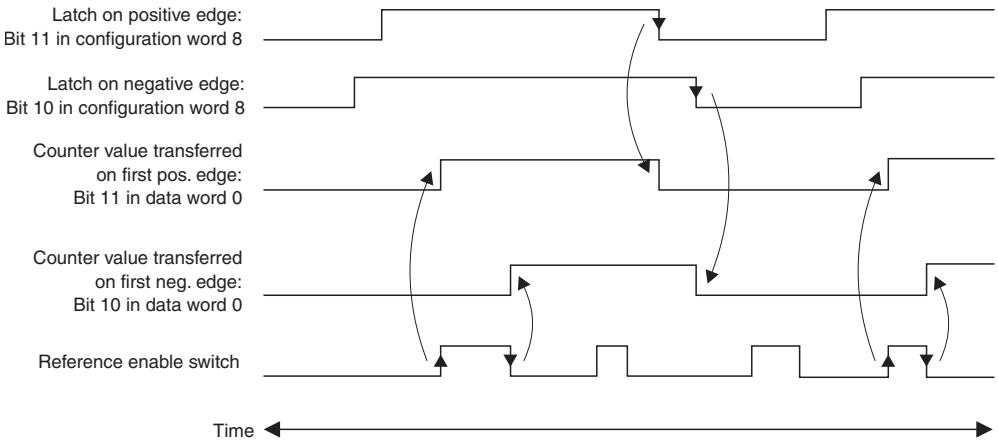
The clock output (pins 7 and 8) correspond to the comparator status of bit 4 in data word 0.

Latching the Counter Value

The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 10 = 0 or 1	Counter value is taken with the first negative edge on the reference enable switch
Configuration word 8	Bit 11 = 0 or 1	Counter value is taken with the first positive edge on the reference enable switch
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram

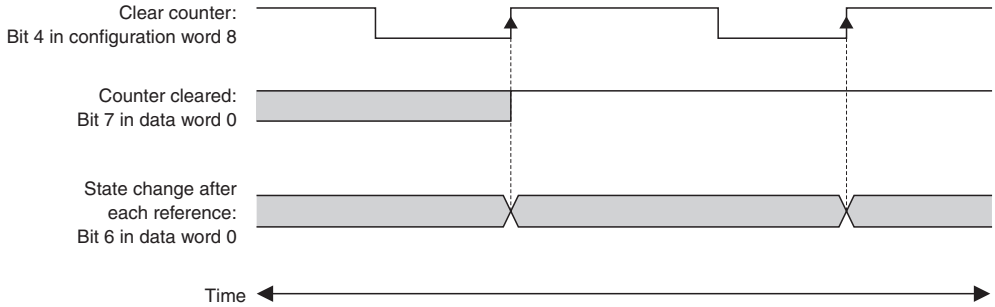


Referencing - Unconditional

The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 4 = 0 or 1	Clear counter (referencing), for control signal see configuration word 14
Configuration word 14	Bit 1 = 0	Clear counter immediately (unconditional referencing)
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram



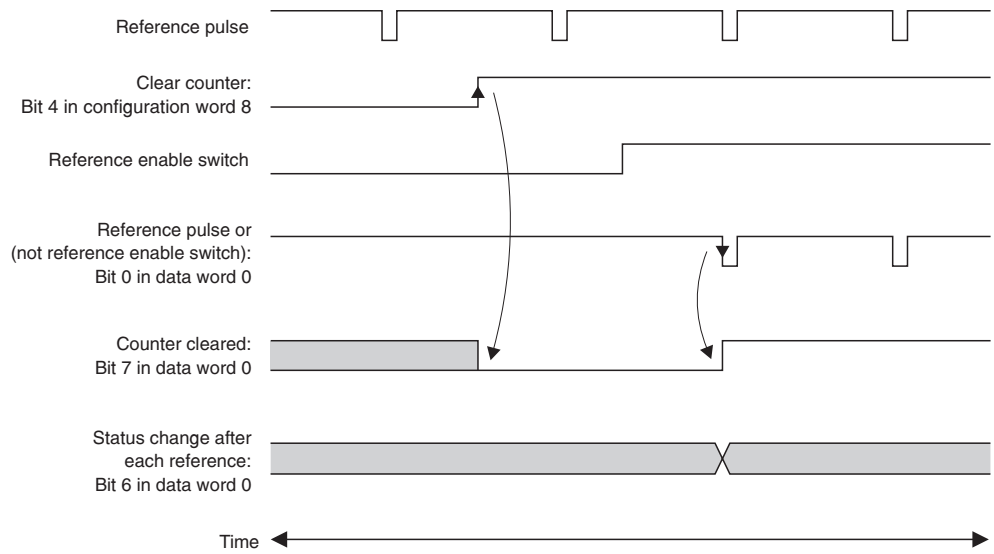
Referencing - Conditional with Reference Enable Switch

Reference pulse - non-inverted

Make the following settings for conditional referencing with reference enable switch and non-inverted reference pulse:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 4 = 0 or 1	Clear counter (referencing), for control signal see configuration word 14
Configuration word 14	Bit 0 = 1	Activate reference enable switch
Configuration word 14	Bit 1 = 1	Conditional referencing
Configuration word 14	Bit 2 = 0	Reference pulse non-inverted
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram

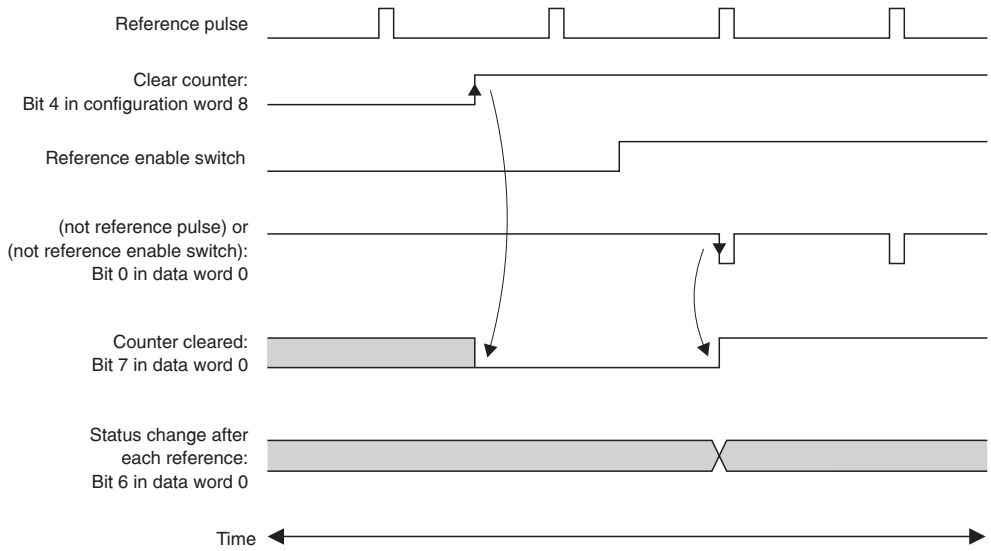


Reference pulse - inverted

Make the following settings for conditional referencing with reference enable switch and inverted reference pulse:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 4 = 0 or 1	Clear counter (referencing), for control signal see configuration word 14
Configuration word 14	Bit 0 = 1	Activate reference enable switch
Configuration word 14	Bit 1 = 1	Conditional referencing
Configuration word 14	Bit 2 = 1	Reference pulse inverted
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram



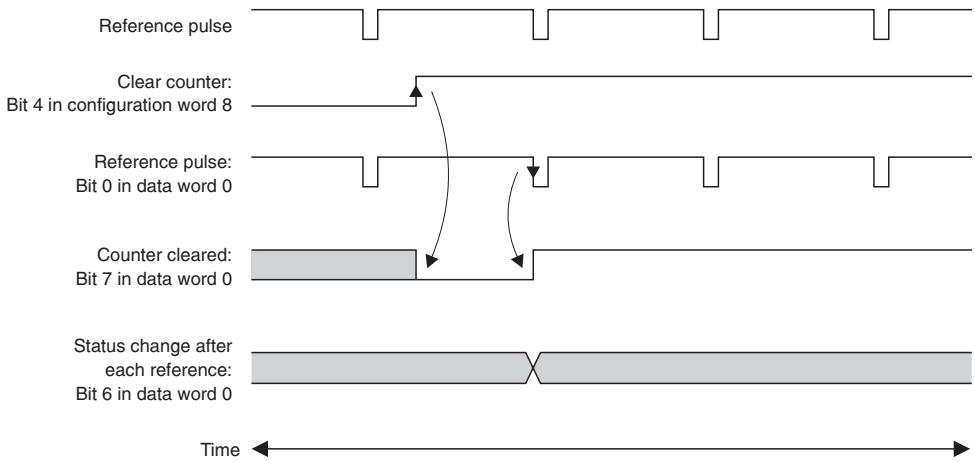
Referencing - Conditional without Reference Enable Switch

Reference pulse - non-inverted

Make the following settings for conditional referencing without reference enable switch and with non-inverted reference pulse:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 4 = 0 or 1	Clear counter (referencing), for control signal see configuration word 14
Configuration word 14	Bit 0 = 0	Ignore reference enable switch
Configuration word 14	Bit 1 = 1	Conditional referencing
Configuration word 14	Bit 2 = 0	Reference pulse non-inverted
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram

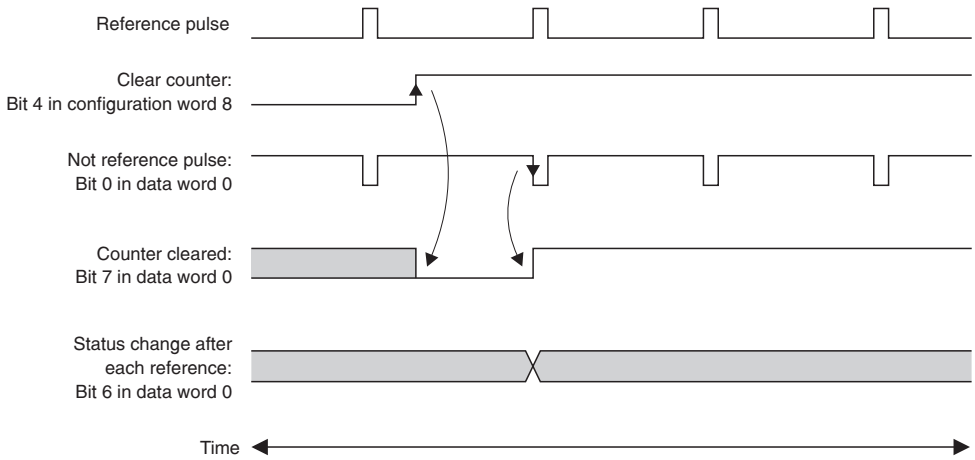


Reference pulse - inverted

Make the following settings for conditional referencing without reference enable switch and with inverted reference pulse:

Data / Configuration Word	Command to be Executed	Description
Configuration word 8	Bit 4 = 0 or 1	Clear counter (referencing), for control signal see configuration word 14
Configuration word 14	Bit 0 = 0	Ignore reference enable switch
Configuration word 14	Bit 1 = 1	Conditional referencing
Configuration word 14	Bit 2 = 1	Reference pulse inverted
Configuration word 14	Bit 12 = 0	Incremental encoder operation

Timing Diagram



15.2.10 Absolute Encoder Operation

In the following examples, the absolute encoder will be read in once in formatted form and once as raw value. The following absolute encoder is used in both examples:

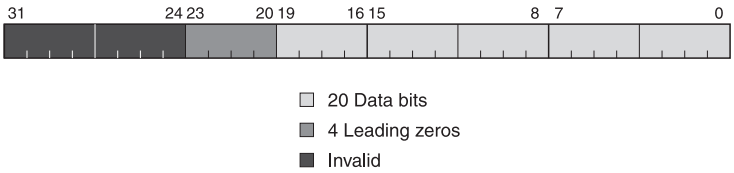
Encoder Type	Multiturn encoder
Encoder Resolution	256 x 4096 ⇒ 20 Bits
Bits Transferred Data Bits Preceding Zeros	24 20 4

Read in formatted data

If the protocol format delivered by the absolute encoder is known, the data is read in in formatted form. The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration word 14	Bit 0 - 4 = %10100	Number of valid bits in the encoder value: 20
Configuration word 14	Bit 5 - 9 = %00100	Number of preceding zeros: 4
Configuration word 14	Bit 11 = 0	Binary coded SSI encoder signal
Configuration word 14	Bit 12 = 1	Absolute encoder operation

Protocol format



Read in data as 32 bit raw value

The data is read in as 32 bit raw value if e.g. the protocol format delivered by the absolute encoder in not known. The following settings are to be made:

Data / Configuration Word	Command to be Executed	Description
Configuration word 14	Bit 0 - 4 = %00000	Number of valid bits in the encoder value: 0
Configuration word 14	Bit 5 - 9 = %00000	Number of preceding zeros: 0
Configuration word 14	Bit 11 = 0	Binary coded SSI encoder signal
Configuration word 14	Bit 12 = 1	Absolute encoder operation

Protocol format