

# X67BC5321

## 1 General information

DeviceNet was developed by Allen-Bradley as a CAN bus based automation network. It is based on a producer/consumer protocol. From the user's point of view, all data is handled completely separately from the features of the CAN bus (e.g. longer data packets are fragmented automatically by DeviceNet). I/O messages with defined characteristics are used for access.

This bus controller makes it possible to connect X2X Link I/O nodes to DeviceNet. It has automatic transfer rate detection, auto scan, automatic mapping and automatic configuration of the I/O modules. Explicit messaging, change of state, cyclic, polled and bit strobe are supported as transfer modes.

In addition to the standard communication objects, there are also vendor-specific objects used to represent the modular X67 system in the best manner possible. X67 and other modules that are based on X2X Link can be connected to the bus controller.

The entire configuration of this type of modular system is supported by the DeviceNet standard. Allen Bradley developed the modular I/O configuration to simplify the necessary configuration steps. The DeviceNet bus controllers from B&R also support this type of configuration.

- Fieldbus: DeviceNet
- 8 digital channels, configurable as inputs or outputs
- Simple I/O configuration via the fieldbus
- Support of both linear and modular (Allen Bradley) configuration systems
- Auto scan, automatic I/O mapping of the I/Os
- Automatic I/O configuration
- Integrated connection to local expansion via X2X Link for 39 additional modules (including up to 16 analog modules)
- 1 ms cycle time for local expansion

### Information:

**Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.**

## 2 Order data


| Model number | Short description   | Figure  |
|--------------|---|---|
|              | <b>Bus controller modules</b>   |   |
| X67BC5321    | X67 bus controller, 1 DeviceNet interface, X2X Link power supply 3 W, 8 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz |  |

Table 1: X67BC5321 - Order data

### Required accessories

See "Required cables and connectors" on page 7.

For a general overview, see section "Accessories - General overview" of the X67 system user's manual.

### 3 Technical data

|  |   |
|--|---|
| <b>Model number</b>                                | <b>X67BC5321</b>  |
| <b>Short description</b>                           |   |
| Bus controller                                     | DeviceNet adapter   |
| <b>General information</b>                         |   |
| Inputs/Outputs                                     | 8 digital channels, configurable as inputs or outputs using software, inputs with additional functions        |
| Isolation voltage between channel and bus          | 500 V <sub>Eff</sub>  |
| Nominal voltage                                    | 24 VDC  |
| B&R ID code  |   |
| Bus controller                                     | 0x17D5  |
| Internal I/O module                                | 0x1311  |
| Sensor/Actuator power supply                       | 0.5 A summation current   |
| Status indicators                                  | I/O function for each channel, supply voltage, bus function   |
| Diagnostics  |   |
| 24 V DeviceNet voltage                             | Yes, with LED status indicators (MOD and NET)   |
| Outputs  | Yes, using status LED and software  |
| I/O power supply                                   | Yes, using status LED and software  |
| Connection type                                    |   |
| Fieldbus   | M12, A-keyed  |
| X2X Link   | M12, B-keyed  |
| Inputs/Outputs                                     | 8x M8, 3-pin  |
| I/O power supply                                   | M8, 4-pin   |
| Power output                                       | 3 W X2X Link power supply for I/O modules   |
| Power consumption                                  |   |
| Fieldbus   | 2.7 W   |
| Internal I/O                                       | 2 W   |
| X2X Link power supply                              | 6.6 W at maximum power output for connected I/O modules   |
| Certifications                                     |   |
| CE   | Yes   |
| KC   | Yes   |
| EAC  | Yes   |
| UL   | cULus E115267<br>Industrial control equipment   |
| HazLoc   | cCSAus 244665<br>Process control equipment<br>for hazardous locations<br>Class I, Division 2, Groups ABCD, T5 |
| ATEX   | Zone 2, II 3G Ex nA IIA T5 Gc<br>IP67, Ta = 0 - Max. 60°C<br>TÜV 05 ATEX 7201X                                |
| <b>Interfaces</b>                                  |   |
| Fieldbus   | DeviceNet adapter   |
| Variant  | M12 interface (male connector on the module)  |
| Max. distance                                      | 500 m   |
| Transfer rate                                      | Max. 500 kbit/s   |
| Default transfer rate                              | Automatic transfer rate detection   |
| Min. cycle time <sup>1)</sup>                      |   |
| Fieldbus   | No limitations  |
| X2X Link   | 400 µs  |
| Synchronization between bus systems possible       | No  |
| Terminating resistor                               | Can be optionally screwed onto the Y-connector  |
| <b>I/O power supply</b>                            |   |
| Nominal voltage                                    | 24 VDC  |
| Voltage range                                      | 18 to 30 VDC  |
| Integrated protection                              | Reverse polarity protection   |
| Power consumption                                  |   |
| Sensor/Actuator power supply                       | Max. 12 W <sup>2)</sup>   |
| <b>Sensor/Actuator power supply</b>                |   |
| Voltage  | I/O power supply minus voltage drop for short circuit protection  |
| Voltage drop for short-circuit protection at 0.5 A | Max. 2 VDC  |
| Summation current                                  | Max. 0.5 A  |
| Short-circuit proof                                | Yes   |
| <b>Digital inputs</b>                              |   |
| Input voltage                                      | 18 to 30 VDC  |
| Input current at 24 VDC                            | Typ. 4 mA   |
| Input characteristics per EN 61131-2               | Type 1  |
| Input filter                                       |   |
| Hardware   | ≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 8)   |
| Software   | Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals  |
| Input circuit                                      | Sink  |
| Additional functions                               | 50 kHz event counting, gate measurement   |
| Input resistance                                   | Typ. 6 kΩ   |

Table 2: X67BC5321 - Technical data

| Model number                                       | X67BC5321  |
|--|--|
| Switching threshold                                |  |
| Low  | <5 VDC   |
| High   | >15 VDC  |
| <b>Event counter</b>                               |  |
| Quantity   | 2  |
| Signal form  | Square wave pulse  |
| Evaluation   | Each falling edge, cyclic counter  |
| Input frequency                                    | Max. 50 kHz  |
| Counter 1  | Input 1  |
| Counter 2  | Input 3  |
| Counter frequency                                  | Max. 50 kHz  |
| Counter size                                       | 16-bit   |
| <b>Gate measurement</b>                            |  |
| Quantity   | 1  |
| Signal form  | Square wave pulse  |
| Evaluation   | Rising edge - Falling edge   |
| Counter frequency                                  |  |
| Internal   | 48 MHz, 3 MHz, 187.5 kHz   |
| Counter size                                       | 16-bit   |
| Length of pause between pulses                     | ≥100 µs  |
| Pulse length                                       | ≥20 µs   |
| Supported inputs                                   | Input 2 or input 4   |
| <b>Digital outputs</b>                             |  |
| Variant  | FET positive switching   |
| Switching voltage                                  | I/O power supply minus residual voltage  |
| Nominal output current                             | 0.5 A  |
| Total nominal current                              | 4 A  |
| Output circuit                                     | Source   |
| Output protection                                  | Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output power supply |
| Diagnostic status                                  | Output monitoring with 10 ms delay   |
| Leakage current when switched off                  | 5 µA   |
| Switching on after overload shutdown               | Approx. 10 ms (depends on the module temperature)  |
| Residual voltage                                   | <0.3 V at 0.5 A rated current  |
| Peak short-circuit current                         | <12 A  |
| Switching delay                                    |  |
| 0 → 1  | <400 µs  |
| 1 → 0  | <400 µs  |
| Switching frequency                                |  |
| Resistive load                                     | Max. 100 Hz  |
| Inductive load                                     | See section "Switching inductive loads"  |
| Braking voltage when switching off inductive loads | 50 VDC   |
| <b>Electrical properties</b>                       |  |
| Electrical isolation                               | Channel isolated from DeviceNet and bus<br>DeviceNet not isolated from bus and channel not isolated from channel                                       |
| <b>Operating conditions</b>                        |  |
| Mounting orientation                               |  |
| Any  | Yes  |
| Installation elevation above sea level             |  |
| 0 to 2000 m  | No limitations   |
| >2000 m  | Reduction of ambient temperature by 0.5°C per 100 m  |
| Degree of protection per EN 60529                  | IP67   |
| <b>Ambient conditions</b>                          |  |
| Temperature  |  |
| Operation  | -25 to 60°C  |
| Derating   | -  |
| Storage  | -40 to 85°C  |
| Transport  | -40 to 85°C  |
| <b>Mechanical properties</b>                       |  |
| Dimensions   |  |
| Width  | 53 mm  |
| Height   | 85 mm  |
| Depth  | 42 mm  |
| Weight   | 200 g  |
| Torque for connections                             |  |
| M8   | Max. 0.4 Nm  |
| M12  | Max. 0.6 Nm  |

Table 2: X67BC5321 - Technical data

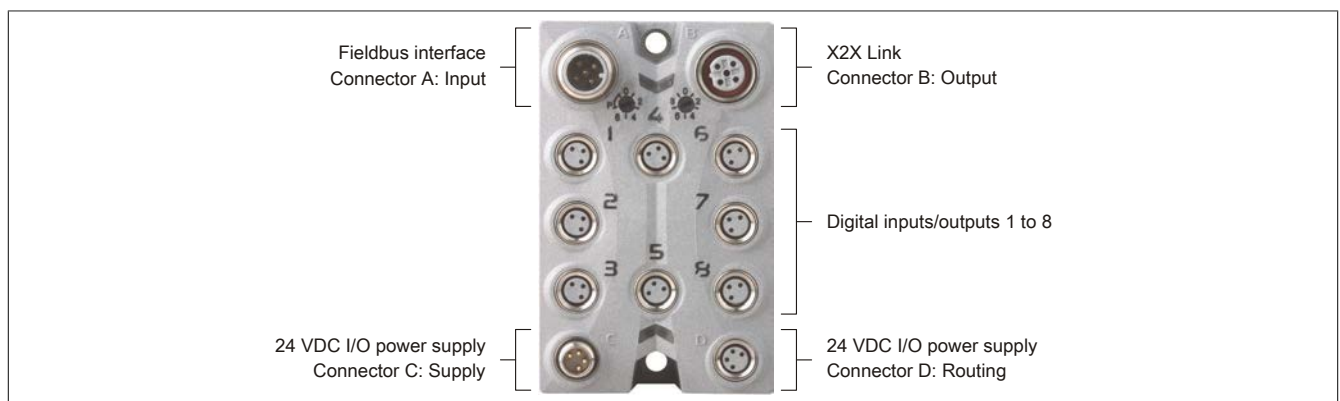
- 1) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
- 2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

### 4 LED status indicators

| Figure  | LED  | Color        | Status  | Description   |  |
|---|--|--------------|---|---|--|
| <p>Status indicator 1:<br/>Left: MOD, Right: NET</p> <p>Status indicator 2:<br/>Left: green, Right: red</p> | <b>Status indicator 1:</b> Status indicator for DeviceNet bus controller |              |   |   |  |
|   | MOD <sup>1)</sup>  | Green        | Off   | No power supply or offline <ul style="list-style-type: none"> <li>• Bus sense error: If LED "MOD" is also off, then there is no 24 V DeviceNet voltage.</li> <li>• No transfer rate<sup>2)</sup></li> </ul>   |  |
|   |  |              | On  | RUN mode<br>The 24 V DeviceNet voltage is OK, and the module is operating under normal conditions.  |  |
|   |  |              | Blinking  | Mode STANDBY<br>Configuration is missing, incomplete or incorrect.  |  |
|   |  | Red          | Blinking  | Mode RECOVERABLE FAULT  |  |
|   |  | Green/Red    | Blinking  | Module is performing a self-test.   |  |
|   | NET <sup>1)</sup>  | Green        | Off   | No power supply or offline: <ul style="list-style-type: none"> <li>• Bus sense error: If LED "MOD" is also off, then there is no 24 V DeviceNet voltage.</li> <li>• No transfer rate<sup>2)</sup></li> <li>• Module has not yet completed a duplicate MAC ID test.</li> </ul> |  |
|   |  |              | Blinking  | Online, not connected: <ul style="list-style-type: none"> <li>• The module has carried out the duplicate MAC- D test and is online.</li> <li>• There is no established connection to a master/scanner.</li> </ul>   |  |
|   |  |              | On  | A connection to the master/scanner (explicit or I/O) has been established.  |  |
|   |  | Red          | Blinking  | A timeout for an I/O connection has occurred.   |  |
|   |  |              | On  | Critical connection error, fieldbus communication no longer possible: <ul style="list-style-type: none"> <li>• Duplicate MAC ID error</li> <li>• Bus off</li> <li>• Receive/Transmit overflow</li> </ul>  |  |
|   | <b>I/O LEDs:</b> Status indicators for I/O channels                      |              |   |   |  |
|   | 1 - 8  | Orange       | -   | Input/Output status of the corresponding channel  |  |
|   | <b>Status indicator 2:</b> Status indicator for module function          |              |   |   |  |
|   | Left   | Green        | Off   | No power to module  |  |
| Single flash  |  |              | RESET mode  |   |  |
| Blinking  |  |              | PREOPERATIONAL mode   |   |  |
| On  |  |              | RUN mode  |   |  |
| Right   | Red  | Off          | No power to module or everything OK   |   |  |
|   |  | On           | Error or reset status   |   |  |
|   |  | Single flash | Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered. |   |  |
|   |  | Double flash | Supply voltage not in the valid range   |   |  |


- 1) The "MOD" and "NET" LEDs are green/red dual LEDs.
- 2) If an LED of status indicator 2 is active (PREOPERATIONAL or RUN mode), the automatic transfer rate detection is still running or no transfer rate could be detected.

### 5 Operating and connection elements



## 6 Fieldbus interface

The bus controller is connected to the fieldbus using pre-assembled cables. The connection is made using M12 circular connectors.

| Connection  | Pinout |   |
|---|--------|---|
|   | Pin    | Description   |
|  | 1      | Shield <sup>1)</sup>                                  |
|   | 2      | 5 V bus power supply                                  |
|   | 3      | CAN <sub>⊥</sub>                                      |
|   | 4      | CAN_High  |
|   | 5      | CAN_Low   |
|   |        | 1) Shield also provided by threaded insert in module. |
| A → A-coded (male), input   |        |   |

### 6.1 Node number

The MAC ID is set using both address switches on the bus controller.

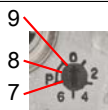
The configurable range is between 0 and 63. This range of values is specified in the DeviceNet specification for a DeviceNet device.



x 10      x 1

| Switch position | MAC ID   |
|-----------------|--|
| 00 to 63        | 0 to 63  |
| 64              | MAC ID setting made via the software configuration                     |
| 65 to 89        | Not permitted  |
| 90              | <a href="#">"Clearing parameters" on page 6</a>                        |
| 91 to 94        | Not permitted  |
| 95              | <a href="#">"Automatic configuration of the I/O modules" on page 7</a> |
| 96 to 99        | Not permitted  |

### Number position in switch position "P"



### Special function

| Position of the address switch | Special function  |
|--------------------------------|---|
| 64                             | With this setting of the address switches, the MAC ID can be set by the master/scanner using software.                          |
| 90                             | Deletes the parameters stored in the bus controller's flash memory. The bus controller is reset back to its factory settings.   |
| 95                             | Completely deletes the old configuration data and overwrites it automatically with the new values of the connected I/O modules. |

### 6.1.1 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received, indicating that the correct transfer rate has been determined. Only transfer rates permitted by the DeviceNet specification are tested.

#### Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate (500 kbit/s), the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

| Transfer rate |
|---------------|
| 500 kbit/s    |
| 250 kbit/s    |
| 125 kbit/s    |

#### Information:

**While automatic transfer rate recognition is running, both DeviceNet LEDs (MOD, NET) are switched off (since there is no LED status definition in the DeviceNet specifications for this status).**

**To ensure that the module has also been supplied with power and booted, this vendor-specific status definition requires that one of the two module I/O status LEDs is active.**

### 6.1.2 Clearing parameters

Various parameters can be stored in the bus controller's flash memory. Deleting these parameters using switch position 90 returns the bus controller to its factory settings.

#### Deleting the parameters

1. Turn off the power supply to the bus controller.
2. Set the node number to 90
3. Turn on the power supply to the bus controller.
4. Wait until the "MOD" LED flashes green for 5 s (3 ms on / 500 ms off). The node number switch "x10" must be set to 0 and then back to 9 within this time window.
5. Wait until the "MOD" LED blinks with a red double-flash (parameters have been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (00 to 63).
8. Turn on the power supply to the bus controller.
9. The bus controller boots with the set node number and automatic transfer rate detection.

### 6.1.3 Automatic configuration of the I/O modules

The automatic configuration of the connected I/O modules by the bus controller is supported starting with Rev. D0 (firmware  $\geq$ V1.23) of the bus controller.

To prevent the configuration data from being accidentally overwritten on the bus controller, the procedure described below must be followed when creating the configuration data. When doing this, it is important that all required I/O modules are also started when booting the bus controller (i.e. supplied with power). This is especially important when using potential groups (E-stop switches).

The automatic configuration sets the following attributes of class 0x65 on the individual I/O modules:

- Module type (0x01)
- Input length (0x03)
- Output length (0x05)

Additional parameters are not set. That means that the connected modules are configured with their standard settings and standard I/O lengths. This can be changed by editing the parameters in the respective master engineering tool.

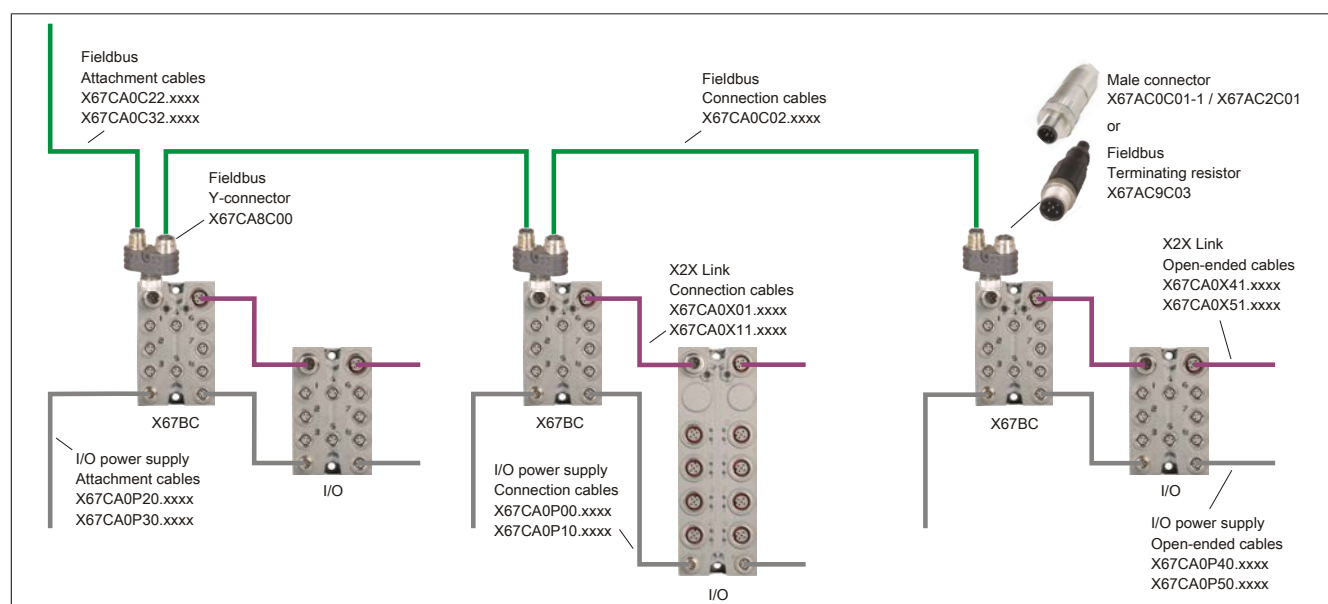
#### Automatic configuration

1. Turn off the power supply to the bus controller.
2. Set node number switch to 95 (this is done by turning switch "x10" to position 9 and switch "x1" to 5).
3. Turn on the power supply to the bus controller.
4. Wait until the "MOD" LED starts blinking green (3 ms on / 500 ms off). This phase of green blinking lasts 5 s. The node number "x10" switch must be set to 0 within this time frame and then set back to 9.
5. Wait until the "MOD" LED blinks (4 red flashes). The old configuration data is now deleted completely and overwritten with the new values from the connected I/O modules.
6. Turn off the power supply to the bus controller.
7. Set the desired node number (00 to 63).
8. Turn on the power supply to the bus controller.
9. The bus controller boots using the set node number, automatic transfer rate recognition and standard settings from the connected I/O modules.

### 6.2 Required cables and connectors


The bus controller is connected to the fieldbus using a Y-connector. This allows the bus controller to be exchanged without interrupting fieldbus communication.

The bus terminating resistor is housed in a connector and screwed onto the Y-connector when needed.



## 7 X2X Link

Additional modules are connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using M12 circular connectors.

| Connection  | Pinout |                  |
|---|--------|------------------|
|   | Pin    | Name             |
|  | 1      | X2X+             |
|   | 2      | X2X              |
|   | 3      | X2X <sub>⊥</sub> |
|   | 4      | X2X <sub>⊥</sub> |
| Shield provided by threaded insert in the module                                  |        |                  |
| B → B-keyed (female), output  |        |                  |



## 8 24 VDC I/O power supply

The I/O power supply is connected via M8 connectors C and D. The power supply is connected via connection C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

### Information:

The maximum permissible current for the I/O power supply is 8 A (4 A per pin).

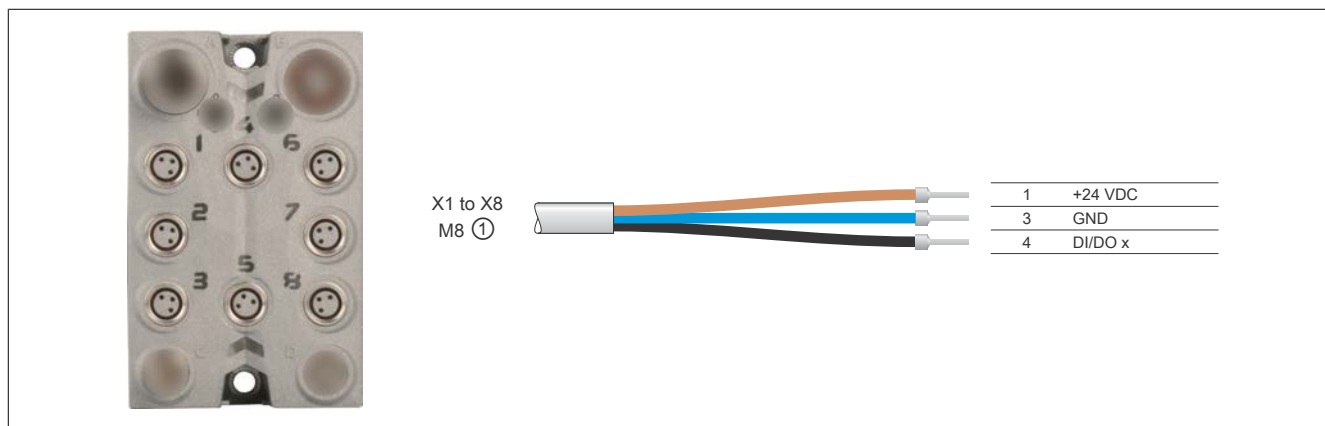
| Connection  | Pinout  |                            |                      |
|---|---|----------------------------|----------------------|
|   | Pin   | Connector C (male)         | Connector D (female) |
|   | 1   | 24 VDC fieldbus / X2X Link | 24 VDC I/O           |
|   | 2   | 24 VDC I/O                 | 24 VDC I/O           |
|   | 3   | GND                        | GND                  |
|   | 4   | GND                        | GND                  |
|  | C → Connector (male) in module, feed for I/O power supply     |                            |                      |
|   | D → Connector (female) in module, routing of I/O power supply |                            |                      |
|   |   |                            |                      |
|   |   |                            |                      |



## 9 Integrated digital mixed module

1 additional mixed module can be saved by the digital mixed module integrated in the bus controller.

### 9.1 Pinout

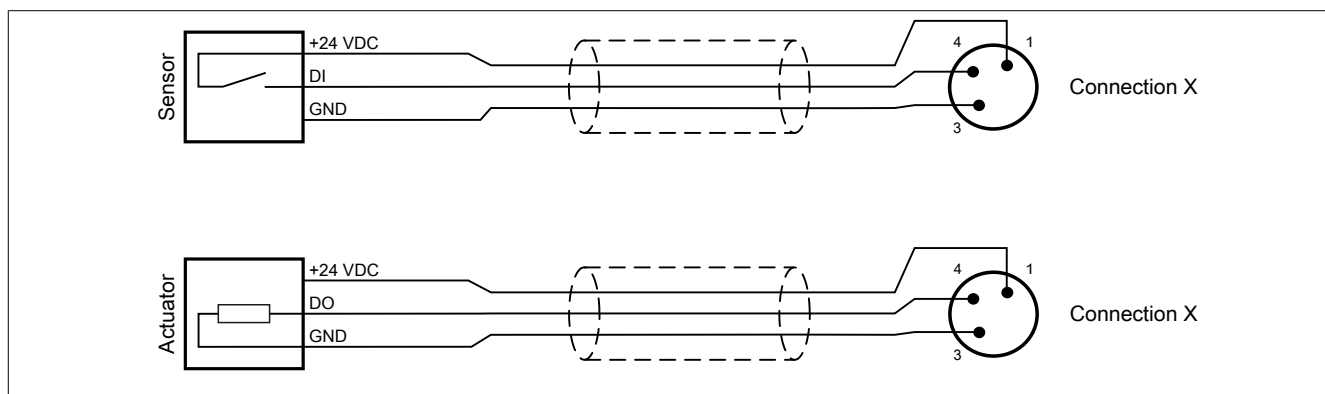


- ① X67CA0D40.xxxx: M8 sensor cable, straight  
X67CA0D50.xxxx: M8 sensor cable, angled

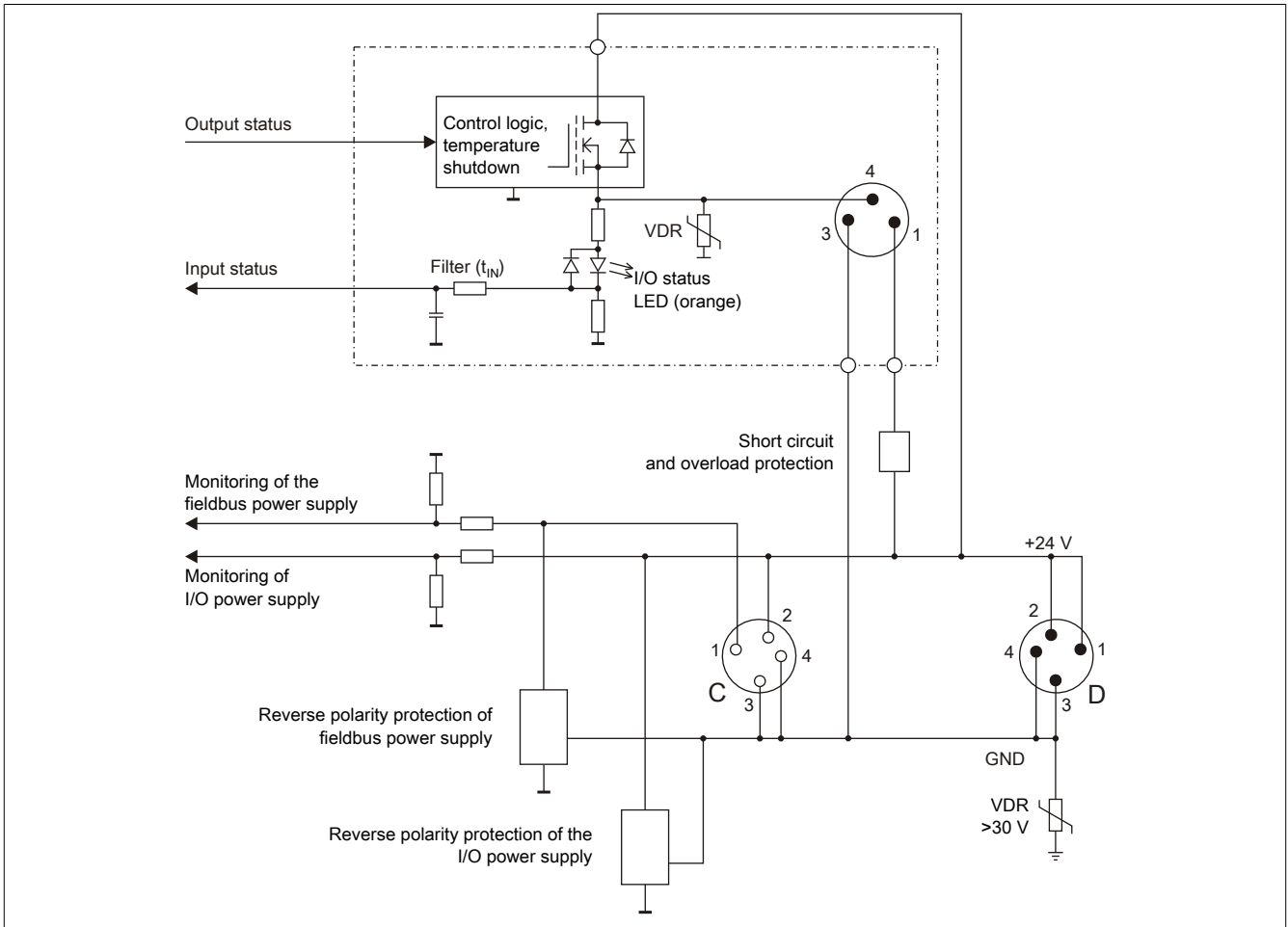
### 9.2 Connections X1 to X8

| M8, 3-pin   | Pinout   |   |      |   |   |   |     |   |                |
|---|--|---|------|---|---|---|-----|---|----------------|
|   | <table border="1"> <thead> <tr> <th>Pin</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>24 VDC sensor/actuator power supply<sup>1)</sup></td> </tr> <tr> <td>3</td> <td>GND</td> </tr> <tr> <td>4</td> <td>Inputs/Outputs</td> </tr> </tbody> </table> | Pin   | Name | 1 | 24 VDC sensor/actuator power supply <sup>1)</sup> | 3 | GND | 4 | Inputs/Outputs |
|   | Pin  | Name  |      |   |   |   |     |   |                |
|   | 1  | 24 VDC sensor/actuator power supply <sup>1)</sup> |      |   |   |   |     |   |                |
|   | 3  | GND   |      |   |   |   |     |   |                |
| 4   | Inputs/Outputs   |   |      |   |   |   |     |   |                |
| 1) Sensors/Actuators are not permitted to be supplied externally. |  |   |      |   |   |   |     |   |                |
| Connections (female), input/output                                |  |   |      |   |   |   |     |   |                |
|   |  |   |      |   |   |   |     |   |                |

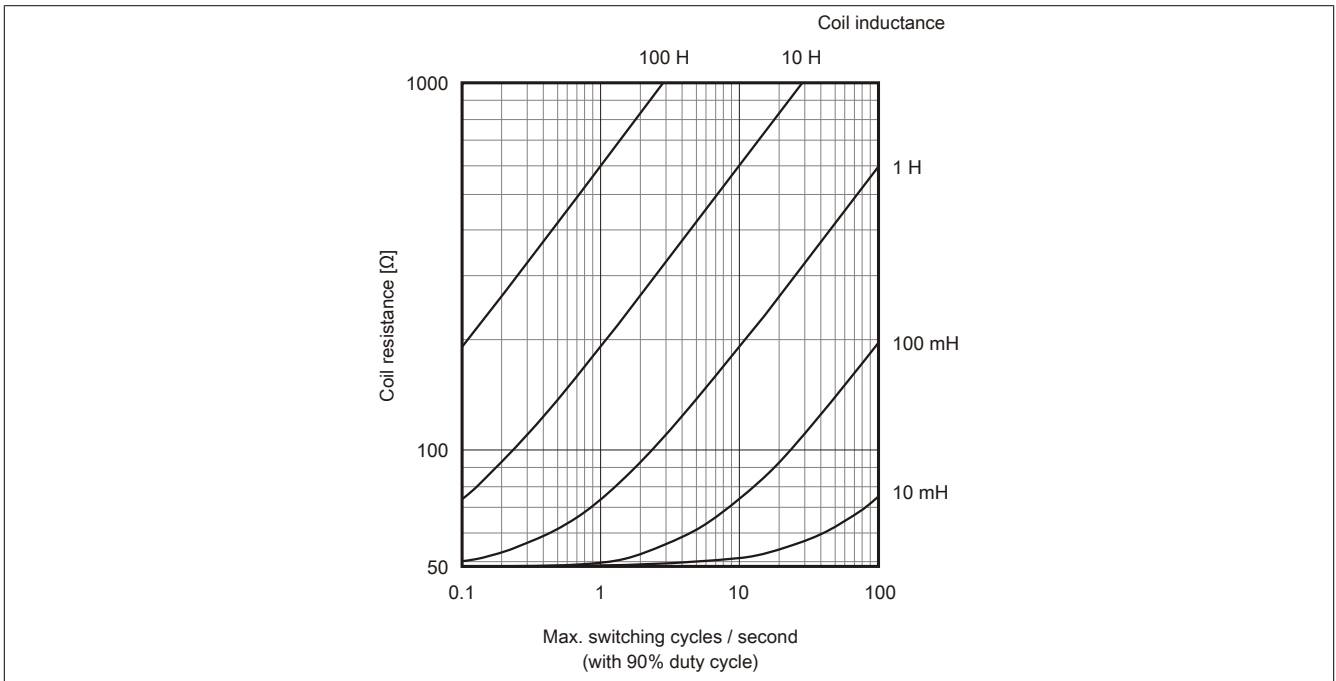
### 9.3 Connection examples



### 9.4 Input/Output circuit diagram



### 9.5 Switching inductive loads



## 10 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available for download from the Downloads section of the B&R website ([www.br-automation.com](http://www.br-automation.com)).

## 11 Register description

### 11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

These general data points are listed in section "Additional information - General data points" of the X67 system user's manual.

### 11.2 Function model 2 - Standard

| Register             | Name                                      | Data type | Read   |         | Write  |         |
|----------------------|---|-----------|--------|---------|--------|---------|
|                      |   |           | Cyclic | Acyclic | Cyclic | Acyclic |
| <b>Configuration</b> |   |           |        |         |        |         |
| 16                   | ConfigIOMask01                            | USINT     |        |         |        | •       |
| 18                   | ConfigOutput03 (input filter)             | USINT     |        |         |        | •       |
| <b>Communication</b> |   |           |        |         |        |         |
| 0                    | Input state of digital inputs 1 to 8      | USINT     | •      |         |        |         |
|                      | DigitalInput01                            | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
| 2                    | DigitalInput08                            | Bit 7     |        |         | •      |         |
|                      | Switching state of digital outputs 1 to 8 | USINT     |        |         |        |         |
|                      | DigitalOutput01                           | Bit 0     |        |         |        |         |
| 30                   | ...                                       | ...       | •      |         |        |         |
|                      | DigitalOutput08                           | Bit 7     |        |         |        |         |
|                      | Status of digital outputs 1 to 8          | USINT     |        |         |        |         |
| 26                   | StatusDigitalOutput01                     | Bit 0     | •      |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | StatusDigitalOutput08                     | Bit 7     |        |         |        |         |
| 28                   | Input latch - Rising edges 1 to 8         | USINT     | •      |         |        |         |
|                      | InputLatch01                              | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
| 8192                 | InputLatch08                              | Bit 7     |        |         | •      |         |
|                      | Acknowledgment - Input latch 1 to 8       | USINT     |        |         |        |         |
|                      | QuitInputLatch01                          | Bit 0     |        |         |        |         |
| 8196                 | ...                                       | ...       |        |         |        |         |
|                      | QuitInputLatch08                          | Bit 7     |        |         |        |         |
|                      | asy_ModulID                               | UINT      |        |         |        |         |
| 8208                 | asy_SupplyInput                           | USINT     |        |         | •      |         |

## 11.3 Function model 1 - Counter

| Register             | Name                                      | Data type | Read   |         | Write  |         |
|----------------------|---|-----------|--------|---------|--------|---------|
|                      |   |           | Cyclic | Acyclic | Cyclic | Acyclic |
| <b>Configuration</b> |   |           |        |         |        |         |
| 16                   | ConfigIOMask01                            | USINT     |        |         |        | •       |
| 20                   | ConfigOutput01 (counter channel 1)        | USINT     |        |         |        | •       |
| 22                   | ConfigOutput02 (counter channel 2)        | USINT     |        |         |        | •       |
| 18                   | ConfigOutput03 (input filter)             | USINT     |        |         |        | •       |
| <b>Communication</b> |   |           |        |         |        |         |
| 0                    | Input state of digital inputs 1 to 8      | USINT     | •      |         |        |         |
|                      | DigitalInput01                            | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | DigitalInput08                            | Bit 7     |        |         |        |         |
| 2                    | Switching state of digital outputs 1 to 8 | USINT     |        |         | •      |         |
|                      | DigitalOutput01                           | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | DigitalOutput08                           | Bit 7     |        |         |        |         |
| 30                   | Status of digital outputs 1 to 8          | USINT     | •      |         |        |         |
|                      | StatusDigitalOutput01                     | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | StatusDigitalOutput08                     | Bit 7     |        |         |        |         |
| 26                   | Input latch - Rising edges 1 to 8         | USINT     | •      |         |        |         |
|                      | InputLatch01                              | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | InputLatch08                              | Bit 7     |        |         |        |         |
| 28                   | Acknowledgment - Input latch 1 to 8       | USINT     |        |         | •      |         |
|                      | QuitInputLatch01                          | Bit 0     |        |         |        |         |
|                      | ...                                       | ...       |        |         |        |         |
|                      | QuitInputLatch08                          | Bit 7     |        |         |        |         |
| 4                    | Counter01                                 | UINT      | •      |         |        |         |
| 6                    | Counter02                                 | UINT      | •      |         |        |         |
| 20                   | Reset counter 1                           | USINT     |        |         | •      |         |
|                      | ResetCounter01                            | Bit 5     |        |         |        |         |
| 22                   | Reset counter 2                           | USINT     |        |         | •      |         |
|                      | ResetCounter02                            | Bit 5     |        |         |        |         |
| 8192                 | asy_ModulID                               | UINT      |        | •       |        |         |
| 8196                 | asy_SupplyStatus                          | USINT     |        | •       |        |         |
| 8208                 | asy_SupplyInput                           | USINT     |        | •       |        |         |

## 11.4 Function model 254 - Bus controller

| Register             | Offset <sup>1)</sup> | Name                                      | Data type | Read   |         | Write  |         |
|----------------------|----------------------|---|-----------|--------|---------|--------|---------|
|                      |                      |   |           | Cyclic | Acyclic | Cyclic | Acyclic |
| <b>Configuration</b> |                      |   |           |        |         |        |         |
| 16                   | -                    | ConfigIOMask01                            | USINT     |        |         |        | •       |
| 20                   | -                    | ConfigOutput01 (counter channel 1)        | USINT     |        |         |        | •       |
| 22                   | -                    | ConfigOutput02 (counter channel 2)        | USINT     |        |         |        | •       |
| 18                   | -                    | ConfigOutput03 (input filter)             | USINT     |        |         |        | •       |
| <b>Communication</b> |                      |   |           |        |         |        |         |
| 0                    | 0                    | Input state of digital inputs 1 to 8      | USINT     | •      |         |        |         |
|                      |                      | DigitalInput01                            | Bit 0     |        |         |        |         |
|                      |                      | ...                                       | ...       |        |         |        |         |
| 2                    | 0                    | DigitalInput08                            | Bit 7     |        |         |        |         |
|                      |                      | Switching state of digital outputs 1 to 8 | USINT     |        |         | •      |         |
|                      |                      | DigitalOutput01                           | Bit 0     |        |         |        |         |
| 30                   | -                    | ...                                       | ...       |        |         |        |         |
|                      |                      | DigitalOutput08                           | Bit 7     |        |         |        |         |
|                      |                      | Status of digital outputs 1 to 8          | USINT     | •      |         |        |         |
| 26                   | -                    | StatusDigitalOutput01                     | Bit 0     |        |         |        |         |
|                      |                      | ...                                       | ...       |        |         |        |         |
|                      |                      | StatusDigitalOutput08                     | Bit 7     |        |         |        |         |
| 28                   | -                    | Input latch - Rising edges 1 to 8         | USINT     | •      |         |        |         |
|                      |                      | InputLatch01                              | Bit 0     |        |         |        |         |
|                      |                      | ...                                       | ...       |        |         |        |         |
| 4                    | -                    | InputLatch08                              | Bit 7     |        |         |        |         |
|                      |                      | Acknowledgment - Input latch 1 to 8       | USINT     |        |         | •      |         |
|                      |                      | QuitInputLatch01                          | Bit 0     |        |         |        |         |
| 6                    | -                    | ...                                       | ...       |        |         |        |         |
|                      |                      | QuitInputLatch08                          | Bit 7     |        |         |        |         |
|                      |                      | Counter01                                 | UINT      |        | •       |        |         |
| 20                   | -                    | Counter02                                 | UINT      |        | •       |        |         |
|                      |                      | Reset counter 1                           | USINT     |        |         | •      |         |
| 22                   | -                    | ResetCounter01                            | Bit 5     |        |         |        |         |
|                      |                      | Reset counter 2                           | USINT     |        |         | •      |         |
| 8192                 | -                    | ResetCounter02                            | Bit 5     |        |         |        |         |
|                      |                      | asy_ModulID                               | UINT      |        | •       |        |         |
| 8196                 | -                    | asy_SupplyStatus                          | USINT     |        | •       |        |         |
| 8208                 | -                    | asy_SupplyInput                           | USINT     |        | •       |        |         |

1) The offset specifies the position of the register within the CAN object.

### 11.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X67 user's manual (version 3.30 or later).

### 11.4.2 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN I/O.

## 11.5 Configuration

### 11.5.1 I/O mask 1 to 8

Name:

ConfigIOMask01

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

#### Information:

In counter operation, channels 1 to 4 can only be configured as inputs.

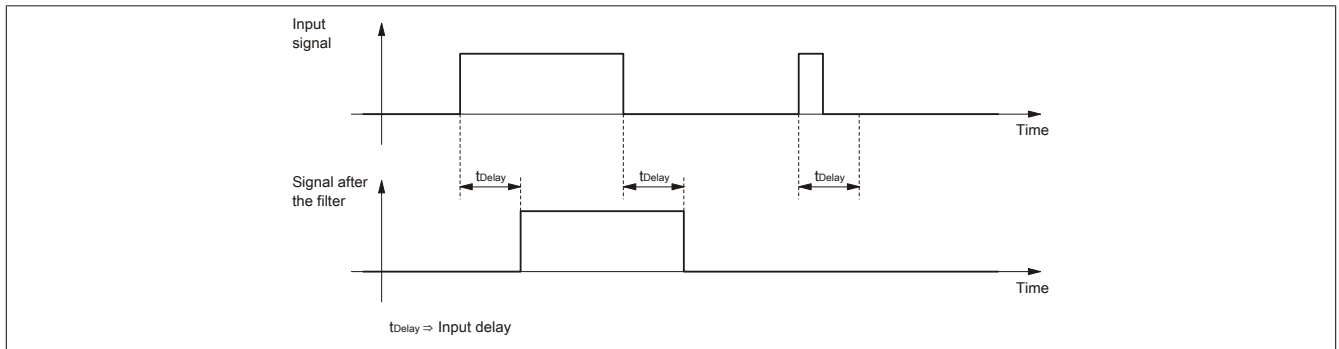
| Data type | Values             | Bus controller default setting |
|-----------|--------------------|--------------------------------|
| USINT     | See bit structure. | 0                              |

Bit structure:

| Bit | Description                          | Value | Information  |
|-----|--------------------------------------|-------|--|
| 0   | Channel 1 configured as input/output | 0     | Configured as input (bus controller default setting) |
|     |                                      | 1     | Configured as output                                 |
| ... | ...                                  | ...   | ...  |
| 7   | Channel 8 configured as input/output | 0     | Configured as input (bus controller default setting) |
|     |                                      | 1     | Configured as output                                 |

### 11.5.2 Input filter

An input filter is available for each input. The input delay can be set using register "[ConfigOutput03](#)" on page 14. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



#### 11.5.2.1 Digital input filter

Name:

ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100  $\mu$ s. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200  $\mu$ s.

| Data type | Value | Filter  |
|-----------|-------|---|
| USINT     | 0     | No software filter (bus controller default setting) |
|           | 2     | 0.2 ms  |
|           | ...   | ...   |
|           | 250   | 25 ms - Higher values are limited to this value     |

### 11.5.3 Configuration of Counter Channels 1 and 2

Name:

ConfigOutput01 to ConfigOutput02

ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

| Data type | Values             | Bus controller default setting |
|-----------|--------------------|--------------------------------|
| USINT     | See bit structure. | 0                              |

Bit structure:

| Bit   | Description   | Value      | Information  |
|-------|---|------------|--|
| 0 - 2 | Configuration of the counter frequency (only with gate measurement) | 000        | Counter frequency = 48 MHz (bus controller default setting)              |
|       |   | 001        | Counter frequency = 3 MHz  |
|       |   | 010        | Counter frequency = 187.5 kHz  |
|       |   | 011 to 111 | Reserved   |
| 3 - 4 | Reserved  | 0          |  |
| 5     | ResetCounter0x  | 0          | No affect on counter (bus controller default setting)                    |
|       |   | 1          | Delete counter   |
| 6 - 7 | Configuration of the operating mode                                 | 0          | <a href="#">Event counter operation</a> (Bus controller default setting) |
|       |   | 1          | <a href="#">Gate measurement</a>   |

#### Event counter operation

The falling edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

#### Gate measurement

##### Information:

**Only one of the counter channels at a time can be used for gate measurement.**

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

### 11.6 Communication

#### 11.6.1 Digital inputs

##### Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

##### Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

##### 11.6.1.1 Input state of digital inputs 1 to 8

Name:

DigitalInput01 to DigitalInput08

This register indicates the input state of digital inputs 1 to 8.

| Data type | Values                 |
|-----------|------------------------|
| USINT     | See the bit structure. |

Bit structure:

| Bit | Name           | Value  | Information                   |
|-----|----------------|--------|-------------------------------|
| 0   | DigitalInput01 | 0 or 1 | Input state - Digital input 1 |
| ... | ...            | ...    | ...                           |
| 7   | DigitalInput08 | 0 or 1 | Input state - Digital input 8 |

## 11.6.2 Digital outputs

The output status is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

### 11.6.2.1 Switching state of digital outputs 1 to 8

Name:

DigitalOutput01 to DigitalOutput08

This register is used to store the switching state of digital outputs 1 to 8.

| Data type | Values                 |
|-----------|------------------------|
| USINT     | See the bit structure. |

Bit structure:

| Bit | Name            | Value | Information             |
|-----|-----------------|-------|-------------------------|
| 0   | DigitalOutput01 | 0     | Digital output 01 reset |
|     |                 | 1     | Digital output 01 set   |
| ... |                 | ...   |                         |
| 7   | DigitalOutput08 | 0     | Digital output 08 reset |
|     |                 | 1     | Digital output 08 set   |

### 11.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

#### 11.6.3.1 Status of digital outputs 1 to 8

Name:

StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

| Data type | Values                 |
|-----------|------------------------|
| USINT     | See the bit structure. |

Bit structure:

| Bit | Name                  | Value | Information                           |
|-----|-----------------------|-------|---------------------------------------|
| 0   | StatusDigitalOutput01 | 0     | Channel 01: No error                  |
|     |                       | 1     | Channel 01: Short circuit or overload |
| ... |                       | ...   |                                       |
| 7   | StatusDigitalOutput08 | 0     | Channel 08: No error                  |
|     |                       | 1     | Channel 08: Short circuit or overload |

### 11.6.4 Input latch

It works in the same way as a dominant reset RS flip-flop.





### 11.6.4.1 Input latch - Rising edges 1 to 8

Name:

InputLatch01 to InputLatch08

The rising edges of the input signal can be latched with a resolution of 200  $\mu$ s in this register. The input latch is either reset or prevented from latching with register "QuitInputLatch0x" on page 17.

| Data type | Values                 |
|-----------|------------------------|
| USINT     | See the bit structure. |

Bit structure:

| Bit | Name         | Value | Information          |
|-----|--------------|-------|----------------------|
| 0   | InputLatch01 | 0     | Do not latch input 1 |
|     |              | 1     | Latch input 1        |
| ... |              | ...   |                      |
| 7   | InputLatch08 | 0     | Do not latch input 8 |
|     |              | 1     | Latch input 8        |

### 11.6.4.2 Acknowledgment - Input latch 1 to 8

Name:

QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

| Data type | Values                 |
|-----------|------------------------|
| USINT     | See the bit structure. |

Bit structure:

| Bit | Name             | Value | Information          |
|-----|------------------|-------|----------------------|
| 0   | QuitInputLatch01 | 0     | Do not reset input 1 |
|     |                  | 1     | Reset input 1        |
| ... |                  | ...   |                      |
| 7   | QuitInputLatch08 | 0     | Do not reset input 8 |
|     |                  | 1     | Reset input 8        |

### 11.6.5 Event counter / Gate measurement

Name:

Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

| Data type | Values     |
|-----------|------------|
| UINT      | 0 to 65535 |

### 11.6.6 Reading the module ID

Name:

asy\_ModulID

This register offers the possibility to read the module ID.

| Data type | Values    |
|-----------|-----------|
| UINT      | Module ID |

### 11.6.7 Operating limit status registers

Name:

asy\_SupplyStatus

This register can be used to read the status of the operating limits.

| Data type | Values             |
|-----------|--------------------|
| USINT     | See bit structure. |

Bit structure:

| Bit   | Description                                    | Value | Information                                    |
|-------|--|-------|--|
| 0     | I/O power supply within/outside warning limits | 0     | Within the warning limits (18 to 30 V)         |
|       |  | 1     | Outside of the warning limits (<18 V or >30 V) |
| 1 - 7 | Reserved                                       | 0     |  |

### 11.6.8 I/O supply voltage

Name:

asy\_SupplyInput

This register contains the I/O supply voltage measured by the module.

| Data type | Values   | Information    |
|-----------|----------|----------------|
| USINT     | 0 to 255 | Resolution 1 V |

### 11.6.9 Output supply voltage

Name:

asy\_SupplyOutput

This register contains the output supply voltage measured by the module.

| Data type | Values   | Information    |
|-----------|----------|----------------|
| USINT     | 0 to 255 | Resolution 1 V |

### 11.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

| Minimum I/O update time |             |
|-------------------------|-------------|
| Without filtering       | 150 $\mu$ s |
| With filtering          | 200 $\mu$ s |
| Counter operation       | 250 $\mu$ s |

### 11.8 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

| Minimum cycle time |             |
|--------------------|-------------|
| Without filtering  | 150 $\mu$ s |
| With filtering     | 200 $\mu$ s |
| Counter operation  | 250 $\mu$ s |