X20RT8381

1 General information

This reACTION Technology module is equipped with 4 high-speed digital inputs and 4 high-speed digital mixed channels. All connections are designed for 1-wire connections. All inputs are designed for sink connections; the outputs are designed for push-pull connections.

A voltage signal of ±10 V can be read or output using 2 analog inputs and 1 analog output, respectively.

Ultrafast reACTION Technology makes it possible to control the integrated I/O channels with response times down to 1 µs. All of the commands that can be used for reACTION programs are provided as function blocks in special libraries (e.g. AsIORTI). Programming in compliance with IEC 61131-3 requirements takes place in the Function Block Diagram editor in Automation Studio.

The module supports blackout mode. In blackout mode, programmable module functionality persists even if the network fails.

- reACTION Technology module
- 4 high-speed digital inputs
- 4 high-speed digital channels, configurable as inputs or outputs
- 2 high-speed analog inputs ±10 V
- 1 high-speed analog output ±10 V
- 1 ABR incremental encoder input 24 V
- Pulse width modulation
- Support of data type "REAL" for arithmetic operations
- Supports blackout mode

2 Order data

Model number	Short description	Figure
	reACTION Technology modules	
X20RT8381	X20 reACTION module, real computing function, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, configurable as inputs or outputs, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution including sign, configurable input filter, 1 analog output ±10 V, 2 µs, 13-bit converter resolution including sign, reACTION Technology module	
	Required accessories	
	Bus modules	
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20RT8381 - Order data

3 Technical data

Model number	X20RT8381
Short description	
I/O module	4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 analog inputs ±10 V, 1 analog output ±10 V, reACTION Technology
General information	
B&R ID code	0xF24E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Inputs	Yes, using status LED and software
Channel type	Yes, using software
reACTION-capable I/O channels	Yes
Blackout mode	
Scope	Module
Function	Programmable
Standalone mode	No
Power consumption	
Bus	0.01 W
Internal I/O	1.7 W
Additional power dissipation caused by actuators (resistive) [W]	+1.1
Type of signal lines [1)]	Shielded cables must be used for all signal lines, cable length: Max. 20 m
Application memory	
Type	64 Mbit flash memory
Data retention	20 years at 55°C
Guaranteed erase/write cycles	100,000
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
Digital inputs	
Quantity	4 inputs and 4 mixed channels, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Input voltage	24 VDC -15% / +20%
Input current at 24 VDC	Typ. 1.3 mA
Input circuit	Sink
Input filter	
Hardware	<3 µs
Software	Default 200 ns, configurable between 200 ns and 5 ms in 10 ns intervals
Connection type	1-wire connections
Input resistance	18.16 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Quantity	2
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Input frequency	Max. 333 kHz
Evaluation	4x
Analog inputs	
Quantity	2 [2)]
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±30 V
Output of digital value during overload	
Undershoot	0x8001
Overshoot	0x7FFF
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 130 kHz

Table 2: X20RT8381 - Technical data

Model number	X20RT8381
Max. error at 25°C	
Gain	0.08% [3]
Offset	0.018% [4]
Max. gain drift	0.003 %/°C [3]
Max. offset drift	0.001 %/°C [4]
Common-mode rejection	
DC	86 dB
50 Hz	84 dB
Common-mode range	±12 V
Nonlinearity	0.015% [4]
Isolation voltage between channel and bus	500 V_{eff}
Sampling frequency	500 kHz
Digital outputs	
Quantity [5]	4 mixed channels, configurable as inputs or outputs using software
Variant	Push-Pull
Nominal voltage	24 VDC
Switching voltage	24 VDC -15% / +20%
Nominal output current	100 mA
Total nominal current	400 mA
Connection type	1-wire connections
Output circuit	Sink or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current")
Diagnostic status	Output monitoring with delay <700 ns
Leakage current when switched off	Approx. 25 µA
$R_{DS(on)}$	140 mΩ
Residual voltage	<0.4 V at nominal current 100 mA
Max. continuous current	100 mA
Peak short-circuit current	<10 A
Switch-on in the event of overload shutdown or short-circuit shutdown	Approx. 3 ms
Switching delay	
0 → 1	<1 µs
1 → 0	<1 µs
Switching frequency	
Resistive load	Min. 50 kHz, max. 500 kHz
Isolation voltage between channel and bus	500 V_{eff}
Analog outputs	
Quantity	1
Output	±10 V
Digital converter resolution	±12-bit
Conversion time	2 µs
Settling time for output changes over entire range	5 µs
Switch on/off behavior	Internal enable relay for startup
Max. error at 25°C	
Gain	0.15% [6]
Offset	0.05% [7]
Output protection	Short circuit protection
Output format	
Data type	INT
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Load per channel	Max. ±10 mA, load ≥1 kΩ
Short-circuit proof	Current limiting ±65 mA
Output filter	1st-order low pass / cutoff frequency 22 kHz
Max. gain drift	0.022 %/°C [6]
Max. offset drift	0.032 %/°C [7]
Error caused by load change	Max. 0.14%, from 10 MΩ → 1 kΩ, resistive
Nonlinearity	0.005% [8]
Isolation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 2: X20RT8381 - Technical data

Model number	X20RT8381
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Derating and hardware configuration"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 2x terminal block X20TB12 separately Order 1x bus module X20BM31 separately
Spacing	$25^{+0.2}$ mm

Table 2: X20RT8381 - Technical data

1) See section "X20 shielding brackets".
2) To reduce power dissipation, B&R recommends bridging unused inputs on the terminal.
3) Based on the current measured value.
4) Based on the 20 V measurement range.
5) See section "Derating and hardware configuration".
6) Based on the current output value.
7) Based on the entire output range.
8) Based on the output range.

4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode or blackout mode
			Double flash	Mode BOOT (during firmware update)[1]
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	e	Red	Off	Module not supplied with power or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring of digital outputs has been triggered.
			Double flash	Supply voltage not in valid range or no reACTION program loaded
			Triple flash	Test of internal memory failed (limited functionality, module must be replaced)
			On	Error or reset state (reACTION program using functions or channels that are not permitted on this hardware)
	e + r	Solid red / Single green flash		Invalid firmware
	1, 2, 5, 6	Green		Input state of the corresponding digital input
	3, 4, 7, 8	Green		Input or output status of the corresponding digital input or output

Table 3: LED status indicators (X1)

1) A firmware update can take several minutes depending on the configuration.

Figure	LED	Color	Status	Description
	1 - 2	Green	Off	Open circuit or disconnected sensor
			Blinking	Input signal overflow or underflow
			On	Analog/Digital converter running, value OK
	1	Orange	Off	Value = 0
			On	Value ≠ 0

Table 4: LED status indicators (X2)

5 Pinout

5.1 X1 - Pinout

To prevent crosstalk, each individual signal line should be shielded. The maximum cable length is 20 m.

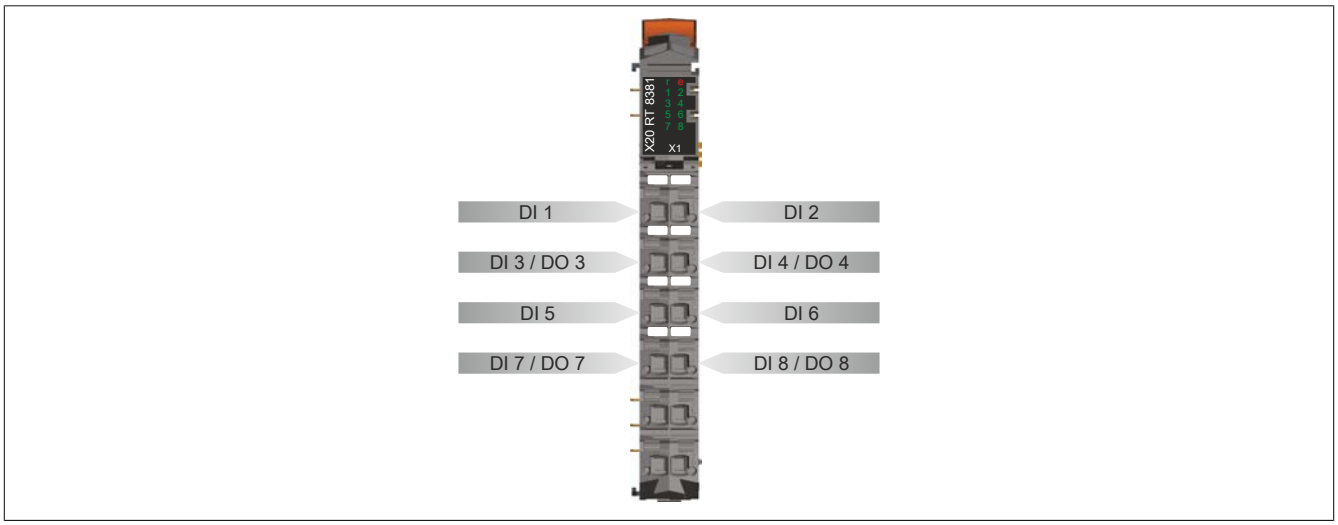


Figure 1: X1 - Pinout

5.2 X2 - Pinout

To prevent crosstalk, each individual signal line should be shielded. The maximum cable length is 20 m.

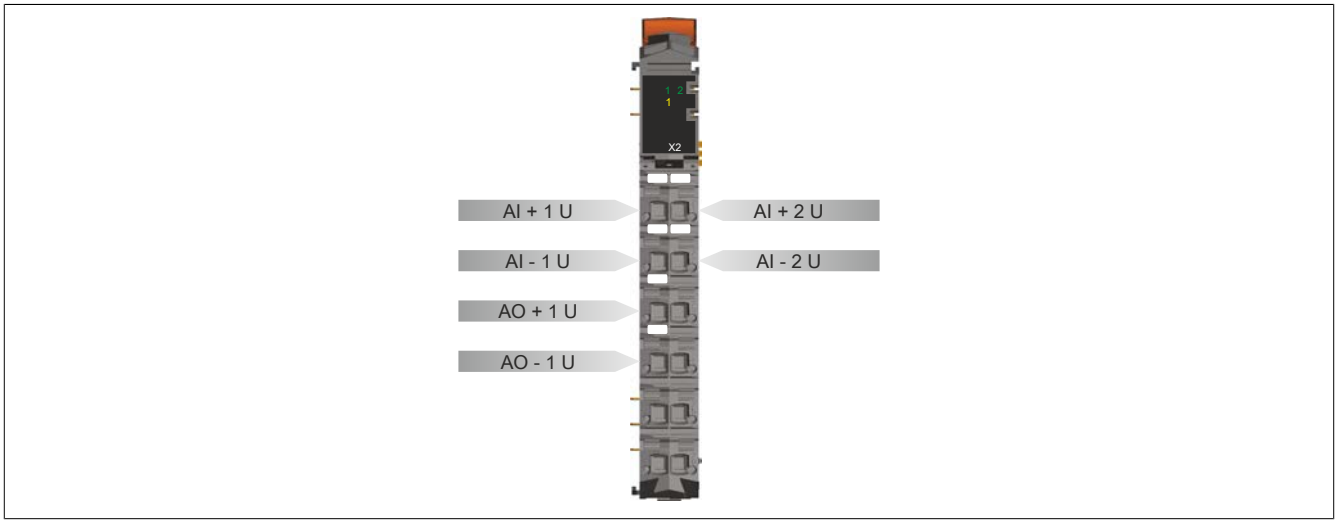


Figure 2: X2 - Pinout

6 Local I/O channels

The following tables provide an overview of the connections to the I/O channels.

Digital inputs/outputs

Connection	Terminal connection	Channel
X1	11	DI 1
	21	DI 2
	12	DI 3 / DO 3
	22	DI 4 / DO 4
	13	DI 5
	23	DI 6
	14	DI 7 / DO 7
	24	DI 8 / DO 8

Analog inputs

Connection	Terminal connection	Channel
X2	11 and 12	AI 1
	21 and 22	AI 2

Analog output

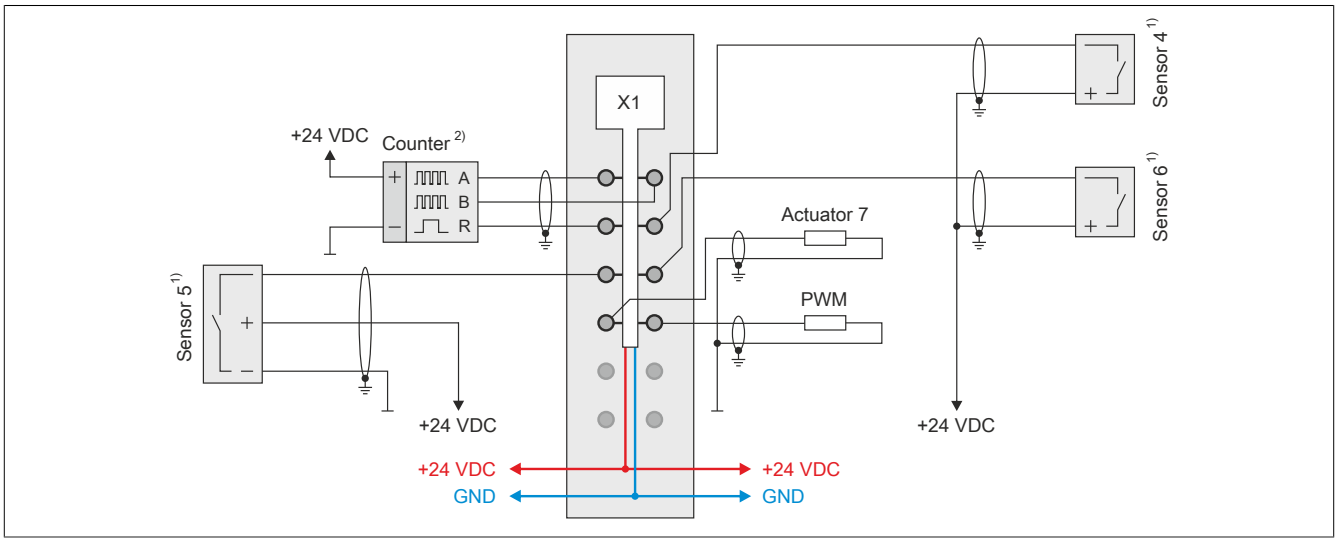
Connection	Terminal connection	Channel
X2	13 and 14	AO 1

The following sections describe assigning I/O channels in a reACTION program:

I/O channels	Assignment
Digital I/O channels	Assignment of digital inputs/outputs
Analog input channels	Assignment of analog inputs
Analog output channel	Assignment of analog output

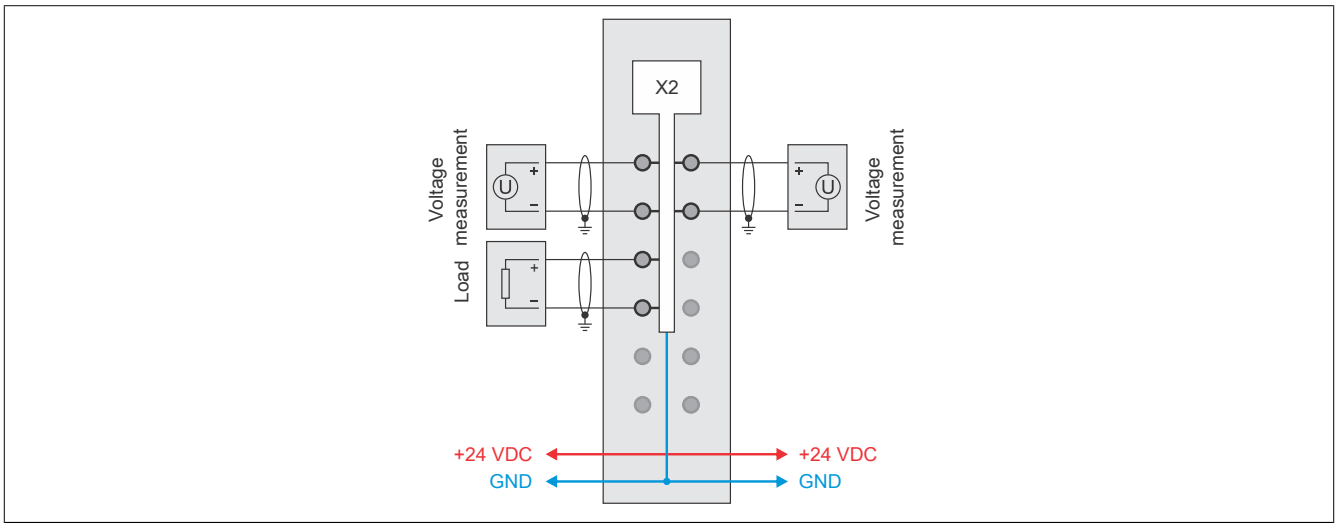
7 Connection examples

7.1 X1 - Connection example



1) Observe the cabling guidelines from the sensor manufacturer.
2) Observe the cabling guidelines from the encoder manufacturer.

7.2 X2 - Connection example



8 Input/Output circuit diagram

8.1 Digital inputs (X1)

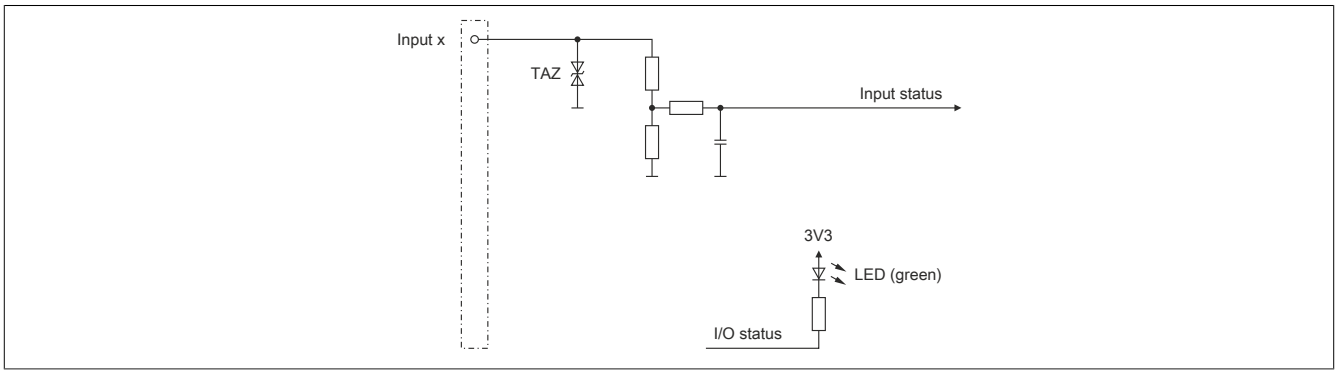


Figure 3: Input circuit diagram of digital inputs (X1)

8.2 Digital mixed channels (X1)

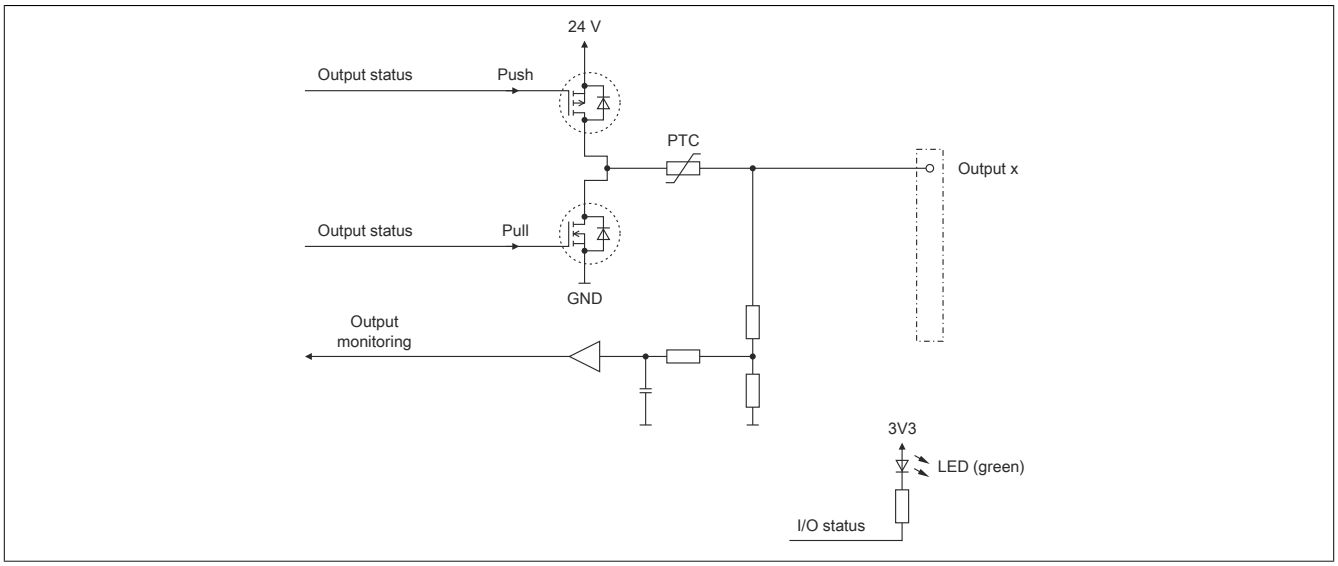


Figure 4: Input/Output circuit diagram of digital mixed channels (X1)

8.3 Analog inputs (X2)

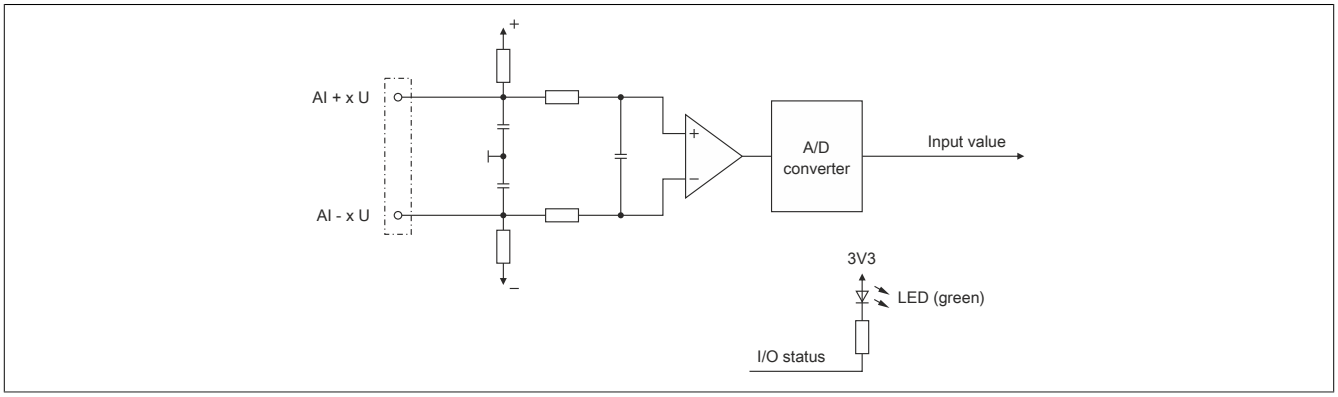


Figure 5: Input circuit diagram of analog inputs (X2)

8.4 Analog output (X2)

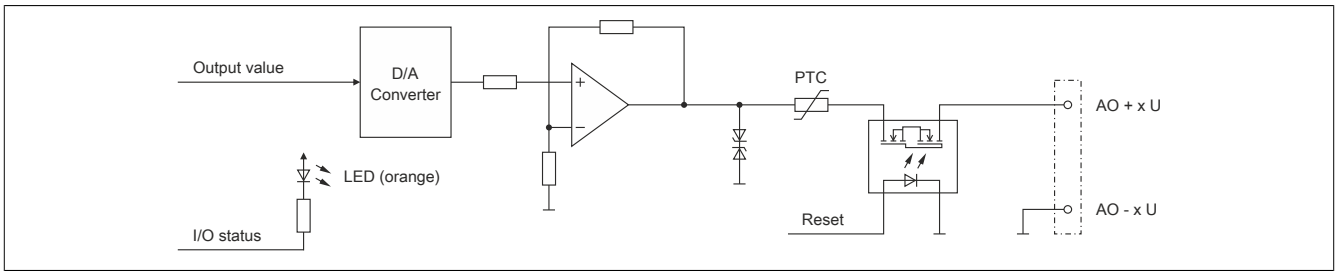


Figure 6: Output circuit diagram of the analog output (X2)

9 Derating and hardware configuration

To ensure proper operation, observe the points listed below:

- Number of operable digital outputs
- Hardware configurations

9.1 Number of operable digital outputs

Depending on the mounting orientation, not all 4 digital outputs of the module can be operated starting at a certain ambient temperature.

> **Information:**
>
> **To ensure operation of the module with the ambient temperatures listed below, it is absolutely necessary to disconnect channels.**
>
> **Reducing the output current per channel does not increase the number of digital output channels that can be operated in the corresponding ambient temperature class.**

Horizontal installation

Ambient temperature	Number of operable digital outputs
<45°C	4
Starting at 45°C	3
Starting at 55°C	2

Vertical installation

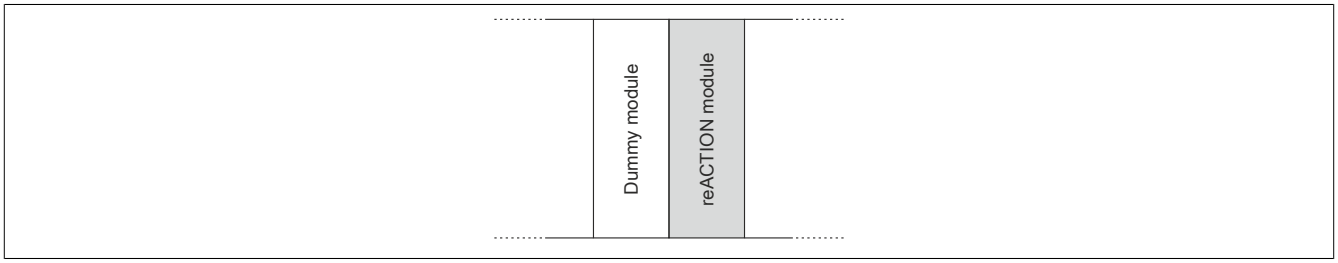
Ambient temperature	Number of operable digital outputs
<35°C	4
Starting at 35°C	3
Starting at 45°C	2

9.2 Hardware configuration for horizontal installation

9.2.1 Hardware configuration starting at an ambient temperature of 50°C

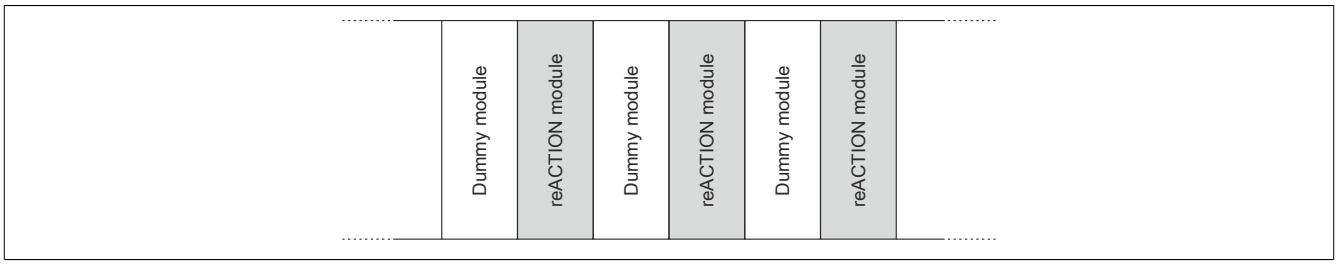
Operating a reACTION module

Starting at an ambient temperature of 50°C, a dummy module must be connected to the left of the reACTION module if installed horizontally.



Operating multiple reACTION modules side by side

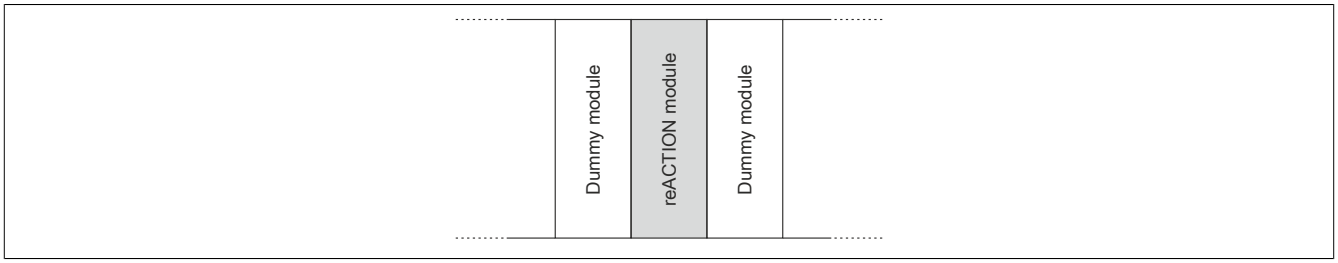
If 2 or more horizontal reACTION modules are being operated in a cluster, the following arrangement of modules must be observed.



9.2.2 Hardware configuration starting at an ambient temperature of 55°C

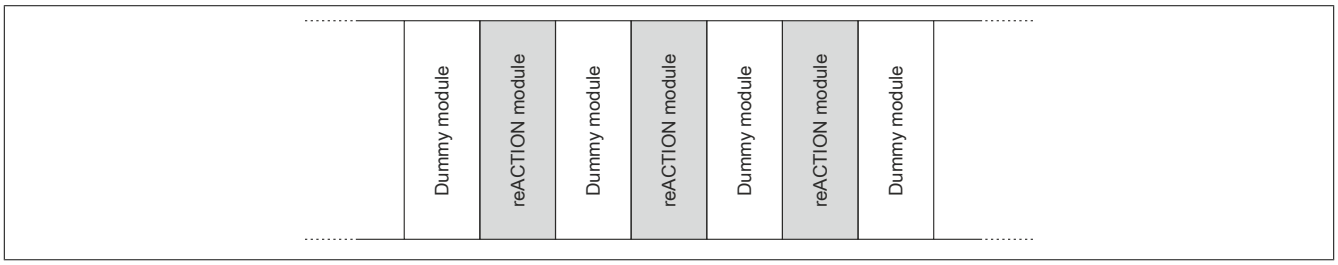
Operating a reACTION module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the reACTION module if installed horizontally.



Operating multiple reACTION modules side by side

If 2 or more horizontal reACTION modules are being operated in a cluster, the following arrangement of modules must be observed.

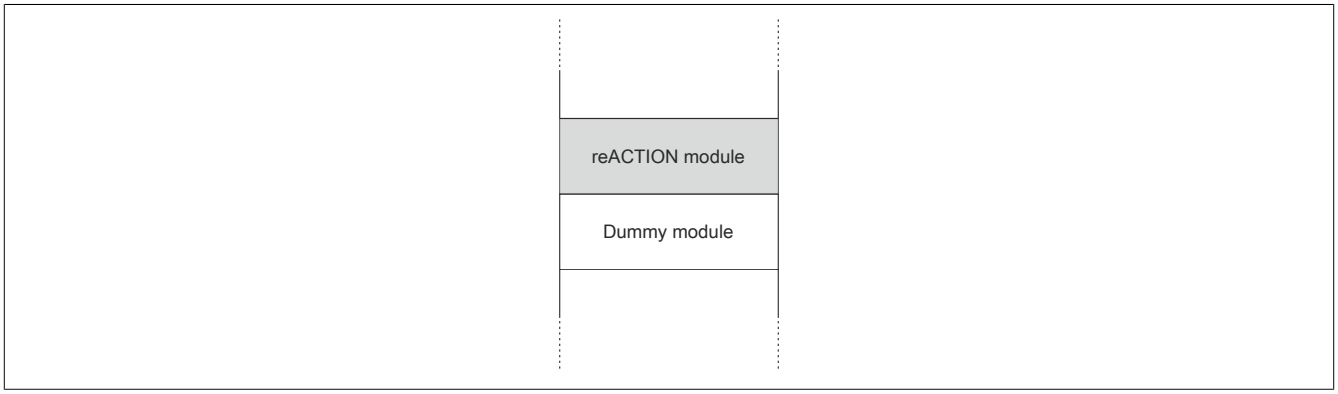


9.3 Hardware configuration for vertical installation

9.3.1 Hardware configuration starting at an ambient temperature of 40°C

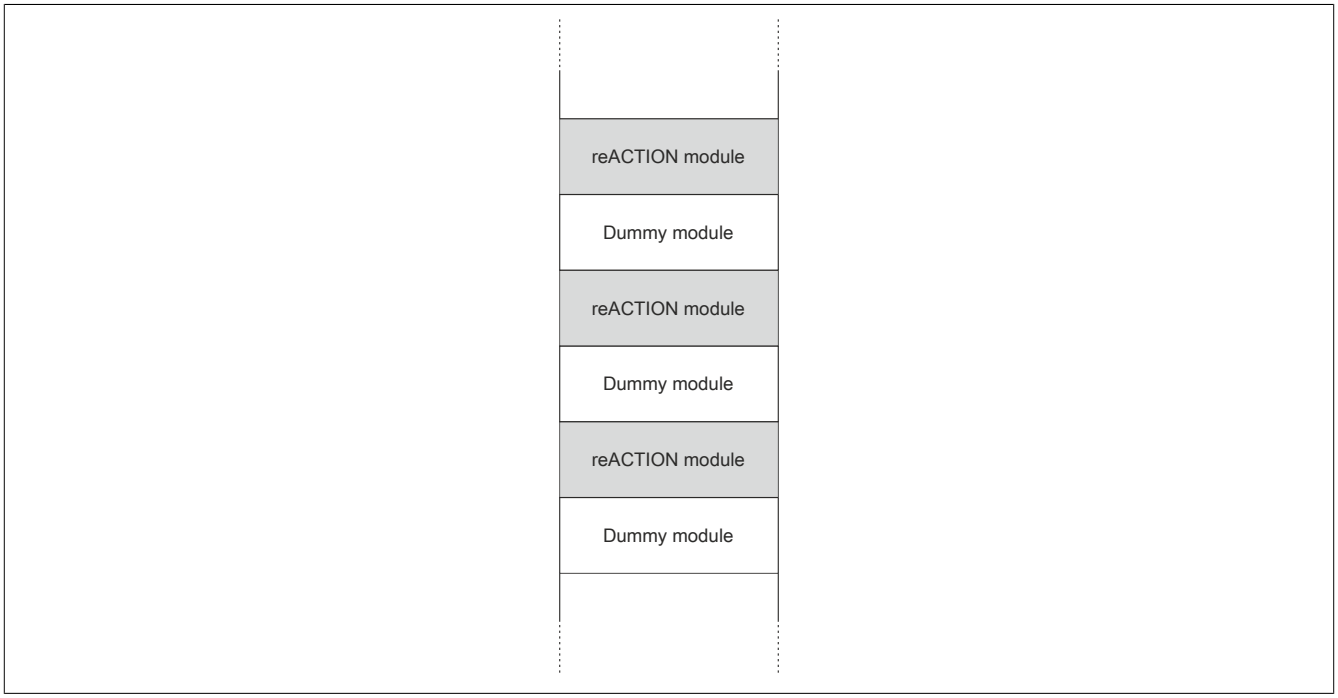
Operating a reACTION module

At ambient temperatures starting at 40°C, a dummy module must be installed below the reACTION module if installed vertically.



Operating multiple reACTION modules side by side

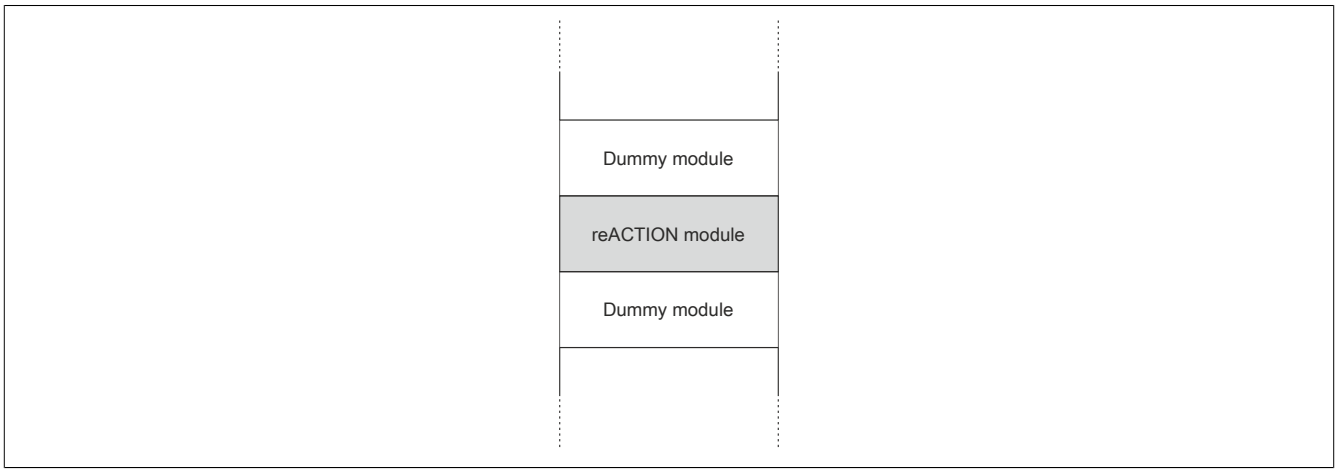
If 2 or more vertical reACTION modules are being operated in a cluster, the following arrangement of modules must be observed.



9.3.2 Hardware configuration starting at an ambient temperature of 45°C

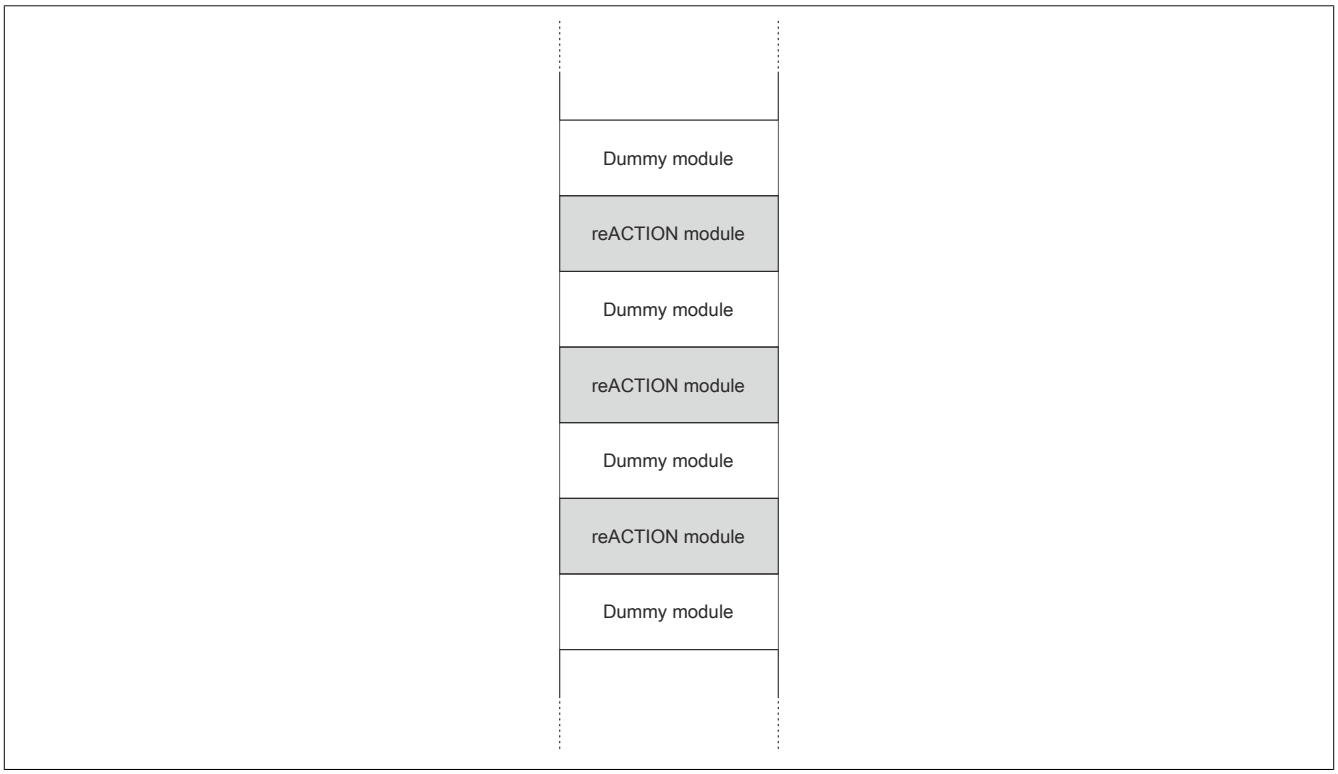
Operating a reACTION module

At ambient temperatures starting at 45°C, dummy modules must be installed above and below the reACTION module if installed vertically.



Operating multiple reACTION modules side by side

If 2 or more vertical reACTION modules are being operated in a cluster, the following arrangement of modules must be observed.



10 Enabling blackout mode

The following steps must be carried out to enable blackout mode.

Requirements

- reACTION program transferred to reACTION module
- Reset triggered on reACTION module:
  This ensures that the program stored in the reACTION memory will be loaded with every subsequent reset.

Enabling

- Set the enable register for blackout mode.
- Control bit "RTEnable" must be set. This bit starts the reACTION engine.

Activation

- A connection error triggers a reset on the reACTION module.
- PAR and VAR data points are set to 0.
- Blackout mode is enabled on the reACTION module.

10.1 Blackout mode

Blackout mode allows users to continue execution of the application in lower-level subsystems if components of the B&R system fail. In this way, the B&R system – independently of redundancy technology – makes it possible to respond to system-critical situations based on the specific application.

The use of blackout-capable modules is recommended for the following requirements:

- Exit routines on system failure, e.g. to enable the opening of a press if the system fails.
- Stopping or controlled setting of an output on system failure, e.g. to automatically close inflow valves.
- Deceleration sequences on system failure, e.g. to reduce motor speeds before transmitting a stop command.

If blackout-capable modules are configured accordingly, blackout mode will be carried out if the network connection to the higher-level controller or CPU is interrupted.

As soon as the network disturbance has been corrected, blackout mode is stopped by the modules and bumpless synchronization with the network takes place.

Requirements for operation

The following requirements must be met in order to use blackout mode:

- The module being used must support blackout mode.
- Parameter "Blackout mode" must be enabled in Automation Studio.

10.1.1 Areas of use

Through the use of blackout-capable modules, a part of the control system can also remain functional if a disturbance in the network or X2X Link connection between the modules occurs.

10.1.1.1 Loss of POWERLINK connection

Initial situation

Several stations in an application are connected to the CPU via network cables. A fault occurs that interrupts data transfer between the CPU and stations.

Effect

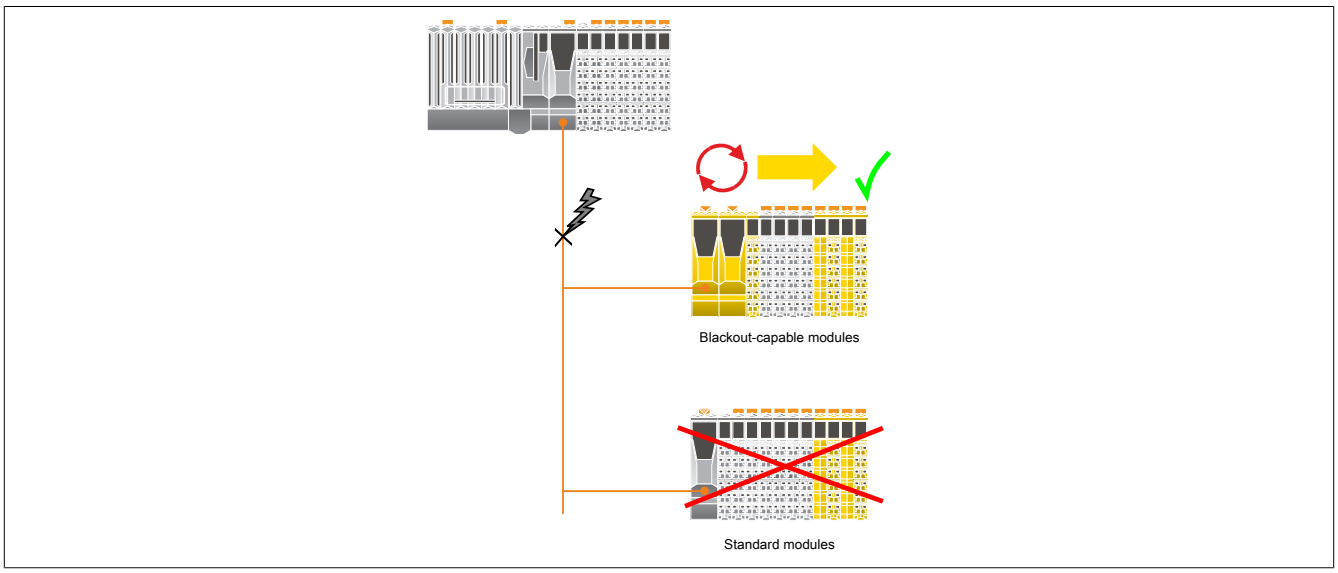
Non-blackout modules are reset and operated according to their default characteristics.

Blackout-capable modules show the following behavior:

- The programmed function continues to be executed.
- Subordinate networks continue to work.
- Data from the CPU is initialized with "0".
- After the disturbance has been corrected, the module bumplessly returns to the higher-level network.

Warning!

Blackout mode causes data from the CPU to be initialized with "0". If blackout mode is used in combination with "output inversion", this can lead to the unwanted setting of outputs.



10.1.1.2 Loss of X2X Link connection

Initial situation

Modules in an application are connected to the network via X2X Link cables. A defect in the X2X Link cable causes the data transfer between the CPU and modules to be interrupted.

Effect

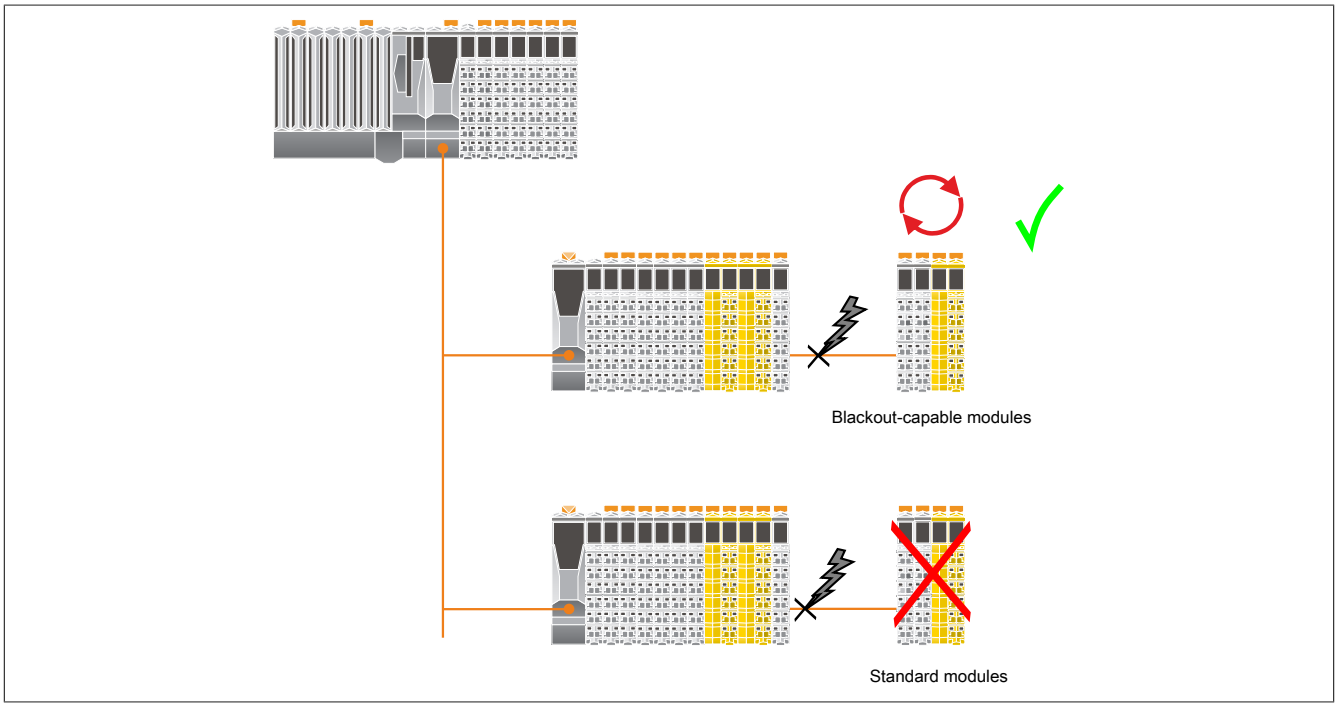
Non-blackout modules are reset and operated according to their default characteristics.

Blackout-capable modules show the following behavior:

- The programmed function continues to be executed.
- Subordinate networks continue to work.
- Data from the CPU is initialized with "0".
- After the disturbance has been corrected, the module bumplessly returns to the higher-level network.

Warning!

Blackout mode causes data from the CPU to be initialized with "0". If blackout mode is used in combination with "output inversion", this can lead to the unwanted setting of outputs.



10.1.2 Programming blackout mode

Blackout mode cannot be detected by the blackout-capable modules themselves. If it is necessary to program specific blackout behavior in an application, an indirect method must therefore be chosen.

One possibility is to implement a counter in the blackout-capable module's higher-level CPU and query it cyclically. Blackout mode would make itself noticeable in this case by a counter value that no longer changes or a counter value of zero.

Blackout-capable modules can be divided into 2 categories:

- **Programmable modules**
  The blackout function is programmed using existing function blocks. In other words, the existing technologies for application programming or reACTION Technology are used.
  The blackout function is executed largely independently of other system components.
- **Standard function modules**
  These modules are not programmable and maintain their default behavior in blackout mode.

11 Register description

11.1 System requirements

The following minimum versions are recommended to generally be able to use all functions:

- Automation Studio 4.4.3
- Automation Runtime 4.08

11.2 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

11.3 Function model 0 - "reACTION"

When using function model "reACTION", a reACTION program must be created specifically for the module. Later, this program will be executed by the reACTION module, not by the CPU. This allows certain machine tasks to be managed decentrally and with a very short response time.

The inputs and outputs of a reACTION module can only be operated by an enabled reACTION program. Interaction registers allow information to be exchanged between the CPU and the reACTION program on the module.

In addition to communication with the CPU, the cyclic interaction registers can also be used for "cross-mapping". In this way, inputs/outputs can also be read/controlled by external modules across the entire X2X Link or POWERLINK network.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module communication						
158	ModuleStatus	UINT		•		
162	DigitalStatus	UINT		•		
166	AnalogInputStatus	UINT		•		
reACTION - Configuration						
772	ReActionCycleTimeValue	UDINT				•
780	ReActionCycleTimeMultiplier	UDINT				•
Index * 8 + 508	CfO_PARType01 to CfO_PARType04	UDINT				•
reACTION - Communication						
129	reACTION - Control byte	USINT			•	
	RTEnable	Bit 0				
	RTHardwareWarningQuit	Bit 2				
145	reACTION - Status byte	USINT	•			
	RTEngineRun	Bit 0				
	RTCycleTimeOverrun	Bit 1				
	RTHardwareWarning	Bit 2				
	RTFileInvalid	Bit 4				
	RTFunctionInvalid	Bit 5				
	RTInstanceInvalid	Bit 6				
	RTFileNotLoaded	Bit 7				
154	RTCycleCounter	UINT	•			
150	RTCycleTime	UINT	•			
reACTION - Interaction						
Index * 8 + 4095	PAR01 to PAR32	(U)SINT			•	
	PAR01_Bit1 to PAR32_Bit1	Bit 0				
	PAR01_Bit2 to PAR32_Bit2	Bit 1				
	PAR01_Bit3 to PAR32_Bit3	Bit 2				
	PAR01_Bit4 to PAR32_Bit4	Bit 3				
	PAR01_Bit5 to PAR32_Bit5	Bit 4				
	PAR01_Bit6 to PAR32_Bit6	Bit 5				
	PAR01_Bit7 to PAR32_Bit7	Bit 6				
	PAR01_Bit8 to PAR32_Bit8	Bit 7				
Index * 8 + 4094	PAR01 to PAR32	(U)INT			•	
Index * 8 + 4092	PAR01 to PAR32	(U)DINT, REAL			•	
Index * 8 + 5119	RES01 to RES32	(U)SINT	•			
	RES01_Bit1 to RES32_Bit1	Bit 0				
	RES01_Bit2 to RES32_Bit2	Bit 1				
	RES01_Bit3 to RES32_Bit3	Bit 2				
	RES01_Bit4 to RES32_Bit4	Bit 3				
	RES01_Bit5 to RES32_Bit5	Bit 4				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	RES01_Bit6 to RES32_Bit6	Bit 5				
	RES01_Bit7 to RES32_Bit7	Bit 6				
	RES01_Bit8 to RES32_Bit8	Bit 7				
Index * 8 + 5118	RES01 to RES32	(U)INT	•			
Index * 8 + 5116	RES01 to RES32	(U)DINT, REAL	•			
Index * 8 + 6140	PVAR1 to PVAR256	DINT, REAL				•
Index * 8 + 6140	RVAR1 to RVAR256	DINT, REAL		•		
reACTION - Function block configuration						
1028	CfO_Config_ABR1	UDINT				•
1036	CfO_ScalingIncrements_ABR1	UDINT				•
1044	CfO_ScalingUnits_ABR1	UDINT				•
1052	CfO_ChannelMapping1_ABR1	UDINT				•
1060	CfO_ChannelMapping2_ABR1	UDINT				•

11.4 Function model 254 - "Direct I/O"

In function model "Direct I/O", a special reACTION program is executed in the module in order to manage the I/O channels. In addition, cyclic registers are used to exchange information with the CPU. This simulates the behavior of a standard module.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module communication						
129	Status - Acknowledgment	USINT			•	
	RTHardwareWarningQuit	Bit 2				
145	Status - Composite message	USINT	•			
	RTHardwareWarning	Bit 2				
159	Status word - Module (L byte)	USINT	•			
	InternalSupplyOk_X1	Bit 1				
	SensorSupplyOk_X2	Bit 2				
	InternalSupplyOk_X2	Bit 3				
	X1ToX2ComError	Bit 6				
	X2ToX1ComError	Bit 7				
157	Status word - Module (H byte)	USINT	•			
	AnalogIn01ComError	Bit 0				
	AnalogIn02ComError	Bit 1				
	AnalogOut01ComError	Bit 4				
163	Status word - Digital (L byte)	USINT	•			
	DigitalOutput3Overload	Bit 2				
	DigitalOutput4Overload	Bit 3				
	DigitalOutput7Overload	Bit 6				
	DigitalOutput8Overload	Bit 7				
167	Status word - AnalogIn (L byte)	USINT	•			
	AnalogIn01Underflow	Bit 0				
	AnalogIn01Overflow	Bit 1				
	AnalogIn01OpenLoop	Bit 2				
169	Status word - AnalogIn (H byte)	USINT	•			
	AnalogIn02Underflow	Bit 0				
	AnalogIn02Overflow	Bit 1				
	AnalogIn02OpenLoop	Bit 2				
Direct I/O - Configuration						
556	CfO_DigitalDirection	UDINT				•
548	CfO_DigitalFilter	UDINT				•
564	CfO_AnalogFilter01	UDINT				•
572	CfO_LowerLimit01	DINT				•
580	CfO_UpperLimit01	DINT				•
588	CfO_AnalogFilter02	UDINT				•
596	CfO_LowerLimit02	DINT				•
604	CfO_UpperLimit02	DINT				•
Direct I/O - Communication						
5	Digital outputs	USINT			•	
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
1	Digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
14	AnalogInput01	INT	•			
18	AnalogInput02	INT	•			
22	AnalogOutput01	INT			•	

11.5 Module communication

11.5.1 Module status messages

Name:
ModuleStatus

This register is used to transfer general status messages for the module.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
Status word - Module (L byte)			
0	Reserved	-	
1	InternalSupplyOk_X1	0	Internal voltage conversion for X1 faulty
		1	No error
2	SensorSupplyOk_X2	0	Power supply for X2 faulty
		1	No error
3	InternalSupplyOk_X2	0	Internal voltage conversion for X2 faulty
		1	No error
4 - 5	Reserved	-	
6	X1ToX2ComError	0	No error
		1	X1 → X2 communication faulty
7	X2ToX1ComError	0	No error
		1	X2 → X1 communication faulty
Status word - Module (H byte)			
0	AnalogIn01ComError	0	No error
		1	Value from analog input 1 faulty
1	AnalogIn02ComError	0	No error
		1	Value from analog input 2 faulty
2 - 3	Reserved	-	
4	AnalogOut01ComError	0	No error
		1	Value from analog output 1 faulty
5 - 7	Reserved	-	

11.5.2 Status messages for the digital channels

Name:
DigitalStatus

This register is used to transfer general status messages for the digital channels.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
Status word - Digital (L byte)			
0 - 1	Reserved	-	
2	DigitalOutput3Overload	0	Digital output 3 OK
		1	Requested voltage 0 V/24 V not achieved
3	DigitalOutput4Overload	0	Digital output 4 OK
		1	Requested voltage 0 V/24 V not achieved
4 - 5	Reserved	-	
6	DigitalOutput7Overload	0	Digital output 7 OK
		1	Requested voltage 0 V/24 V not achieved
7	DigitalOutput8Overload	0	Digital output 8 OK
		1	Requested voltage 0 V/24 V not achieved

11.5.3 Status messages from analog inputs

Name:
AnalogInputStatus

This register transfers general status messages of analog inputs.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
Status word - AnalogIn (L byte)			
0	AnalogIn01Underflow	0	No error
		1	Lower limit value from analog input 1 underrun
1	AnalogIn01Overflow	0	No error
		1	Upper limit value from analog input 1 exceeded
2	AnalogIn01OpenLoop	0	No error
		1	Open circuit determined on analog input 1
3 - 7	Reserved	-	
Status word - AnalogIn (H byte)			
0	AnalogIn02Underflow	0	No error
		1	Lower limit value from analog input 2 underrun
1	AnalogIn02Overflow	0	No error
		1	Upper limit value from analog input 2 exceeded
2	AnalogIn02OpenLoop	0	No error
		1	Open circuit determined on analog input 2
3 - 7	Reserved	-	

11.6 reACTION - Configuration

11.6.1 reACTION cycle time

Name:
ReActionCycleTimeValue
ReActionCycleTimeMultiplier

Registers "TimeValue" and "Multiplier" predefine the desired cycle time for the reACTION program. Register "TimeValue" contains the value, while register "Multiplier" contains the associated units.
Register "Multiplier" is currently permanently set to 1000 in order to predefine the cycle time with µs precision.

Data type	Value
UDINT	1 to 10000

11.6.2 Configuring PAR data points

Name:
CfO_PARType01
CfO_PARType[02...04]

PAR data points can be defined for the reACTION program. To enable them, the desired data type must be made known according to the configuration in Automation Studio.

Data type	Value
UDINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Type01 - PAR 1 Type02 - PAR 9 Type03 - PAR 17 Type04 - PAR 25	0000	Inactive
		0001	USINT, BOOL
4 - 7	Type01 - PAR 2 Type02 - PAR 10 Type03 - PAR 18 Type04 - PAR 26	0010	UINT
		0011	UDINT, REAL
8 - 11	Type01 - PAR 3 Type02 - PAR 11 Type03 - PAR 19 Type04 - PAR 27	0100	Reserved
		0101	SINT
12 - 15	Type01 - PAR 4 Type02 - PAR 12 Type03 - PAR 20 Type04 - PAR 28	0110	INT
		0111	DINT
16 - 19	Type01 - PAR 5 Type02 - PAR 13 Type03 - PAR 21 Type04 - PAR 29	1000 … 1111	Reserved
20 - 23	Type01 - PAR 6 Type02 - PAR 14 Type03 - PAR 22 Type04 - PAR 30		
24 - 27	Type01 - PAR 7 Type02 - PAR 15 Type03 - PAR 23 Type04 - PAR 31		
28 - 31	Type01 - PAR 8 Type02 - PAR 16 Type03 - PAR 24 Type04 - PAR 32		

11.7 reACTION - Communication

At runtime, the reACTION module program is controlled via the program sequence in the CPU. In its active state, the reACTION program is then executed independently of the program sequence in the CPU.

11.7.1 Controlling the reACTION module

Name:
RTEnable
RTHardwareWarningQuit

This register controls the reACTION program.

Data type	Value
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	RTEnable	0	Stops the reACTION program
		1	Starts the reACTION program
1	Reserved	-	
2	RTHardwareWarningQuit	0	No effect
		1	Acknowledges warning messages for the inputs and outputs
3 - 7	Reserved	-	

11.7.2 reACTION module status messages

Name:
RTEngineRun
RTCycleTimeOverrun
RTHardwareWarning
RTFileInvalid
RTFunctionInvalid
RTInstanceInvalid
RTFileNotLoaded

This register is used to output various status messages.

Data type	Value
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	RTEngineRun	0	reACTION program inactive
		1	reACTION program active
1	RTCycleTimeOverrun	0	Configured RT cycle time observed
		1	RT cycle time set too short
2	RTHardwareWarning (group bit for acyclic status data points)	0	No status messages
		1	Warning message for the inputs and outputs
3	Reserved	-	
4	RTFileInvalid (invalid RT program preloaded)	0	RT program in RAM OK
		1	RT program in RAM invalid
5	RTFunctionInvalid (invalid software function)	0	RT program OK
		1	RT program requesting invalid function block
6	RTInstanceInvalid (invalid hardware instance)	0	RT program OK
		1	RT program requesting invalid I/O
7	RTFileNotLoaded	0	Valid RT program in RT engine
		1	No RT program loaded

11.7.3 Cycle counter for the active reACTION program

Name:
RTCycleCounter

Register "CycleCounter" can be used to determine how often the reACTION program has cycled.

Data type	Value
UINT	0 to 65535

11.7.4 Minimum cycle time of the active reACTION program

Name:
RTCycleTime

Register "RTCycleTime" can be used to determine how much time the reACTION module needs to cycle through the loaded program once.

Data type	Value
UINT	0 to 65535: Units 10 ns

11.8 reACTION - Interaction

After startup, the reACTION program in the module runs independently. It reads the images of the required inputs and manages its assigned outputs throughout the entire network. In addition, the reACTION program can interact with the CPU. There are 3 different data point types available for this.

11.8.1 PAR data points

Name:
PAR[01...32]
PAR[01...32]_Bit1
PAR[01...32]_Bit2
PAR[01...32]_Bit3
PAR[01...32]_Bit4
PAR[01...32]_Bit5
PAR[01...32]_Bit6
PAR[01...32]_Bit7
PAR[01...32]_Bit8

Once enabled, the PAR data points are transported cyclically via X2X Link. They are used to transfer information from the CPU to the reACTION program. They can be used to intervene in the execution of the reACTION program.

Information:

PAR data points DO NOT control the module's outputs directly!

Data type	Value
(U)SINT, BOOL	Corresponding range of values
(U)INT	
(U)DINT	

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
4095 + Index * 8	PAR01 PAR[02...32]	(U)SINT			•	
	PAR01_Bit1 PAR[02...32]_Bit1	Bit 0				
	PAR01_Bit2 PAR[02...32]_Bit2	Bit 1				
	PAR01_Bit3 PAR[02...32]_Bit3	Bit 2				
	PAR01_Bit4 PAR[02...32]_Bit4	Bit 3				
	PAR01_Bit5 PAR[02...32]_Bit5	Bit 4				
	PAR01_Bit6 PAR[02...32]_Bit6	Bit 5				
	PAR01_Bit7 PAR[02...32]_Bit7	Bit 6				
	PAR01_Bit8 PAR[02...32]_Bit8	Bit 7				
4094 + Index * 8	PAR01 PAR[02...32]	(U)INT			•	
4092 + Index * 8	PAR01 PAR[02...32]	(U)DINT, REAL			•	

11.8.2 RES data points

Name:
RES[01...32]
RES[01...32]_Bit1
RES[01...32]_Bit2
RES[01...32]_Bit3
RES[01...32]_Bit4
RES[01...32]_Bit5
RES[01...32]_Bit6
RES[01...32]_Bit7
RES[01...32]_Bit8

Once enabled, the RES data points are transported cyclically via X2X Link. They are used to transfer information from the reACTION program to the CPU.

Information:

RES data points DO NOT map the module's input directly!

Data type	Value
(U)SINT, BOOL	Corresponding range of values
(U)INT	
(U)DINT	

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
5119 + Index * 8	RES01 RES[02...32]	(U)SINT	•			
	RES01_Bit1 RES[02...32]_Bit1	Bit 0				
	RES01_Bit2 RES[02...32]_Bit2	Bit 1				
	RES01_Bit3 RES[02...32]_Bit3	Bit 2				
	RES01_Bit4 RES[02...32]_Bit4	Bit 3				
	RES01_Bit5 RES[02...32]_Bit5	Bit 4				
	RES01_Bit6 RES[02...32]_Bit6	Bit 5				
	RES01_Bit7 RES[02...32]_Bit7	Bit 6				
	RES01_Bit8 RES[02...32]_Bit8	Bit 7				
5118 + Index * 8	RES01 RES[02...32]	(U)INT	•			
5116 + Index * 8	RES01 RES[02...32]	(U)DINT, REAL	•			

11.8.3 PVAR and RVAR data points

Name:
PVAR[1...256]
RVAR[1...256]

In addition to PAR and RES data points, VAR data points can also be defined in the reACTION program. They are a direct component of the reACTION program and can be accessed acyclically by the CPU. Like the PAR and RES data points, PVAR data points are used to transfer information from the CPU to the reACTION program. RVAR data points are used to transfer feedback from the reACTION program to the CPU.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
6140 + Index * 8	PVAR1 PVAR[2...256]	DINT, REAL				•
6140 + Index * 8	RVAR1 RVAR[2...256]	DINT, REAL		•		

11.9 reACTION function blocks - General

The following tables provide an overview of I/O channel assignments to reACTION function blocks.

Digital inputs/outputs

Channel	Function block		
	Mapping[1)]	rtiDin	rtiDout, rtiDoutTime
X1: DI 1	0x00	Channel 1	
X1: DI 2	0x01	Channel 2	
X1: DI 3 / DO 3	0x02	Channel 3	Channel 3
X1: DI 4 / DO 4	0x03	Channel 4	Channel 4
X1: DI 5	0x04	Channel 5	
X1: DI 6	0x05	Channel 6	
X1: DI 7 / DO 7	0x06	Channel 7	Channel 7
X1: DI 8 / DO 8	0x07	Channel 8	Channel 8

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 29).

Analog inputs

Channel	Function block		
	Mapping[1)]	rtiAin	rtiAout
X2: AI 1	0x00	Channel 1	
X2: AI 2	0x01	Channel 2	

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 29).

Analog output

Channel	Function block		
	Mapping[1)]	rtiAin	rtiAout
X2: AO 1	0x00		Channel 1

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 29).

11.10 reACTION function blocks - Configuration

Some function blocks in library AsIoRti must be configured before they can be used.

Function block	Information
rtiABRPos	The module offers the option of using function block rtiABRPos once in the reACTION program. To do so, the function block must be assigned 3 digital inputs that are no longer available for rtiDin.
rtiABCnt	The module offers the option of using function block rtiABCnt up to 3 times in the reACTION program. To do so, the function blocks must be assigned 2 digital inputs as an A or B track that are no longer available for rtiDin. In addition, an external event can be defined for each rtiABCnt function block. The input used for this is also no longer available for rtiDin.

Table 5: List of function blocks requiring prior configuration

11.10.1 Function blocks rtiABRPos and rtiABCnt

Function blocks rtiABRPos and rtiABCnt can be used to process the position value of an ABR incremental encoder in a reACTION task. Several hardware channels of the module are used for this. The incoming signals are interpreted by the reACTION engine and converted into a location.

The update rate depends on both the reACTION engine and the hardware used. The reACTION engine is basically able to calculate positions with an update rate of up to 8 MHz. The input frequencies of the hardware inputs can be taken from the technical data of the respective module.

These function blocks can be used separately or in combination.

Using function block rtiABRPos

The following points are important to keep in mind when using function block rtiABRPos in a reACTION program:

- The function block can only be used once in a reACTION program.
- 3 digital inputs must be defined on the module for input signals A, B and R.
- In addition, a digital input of the module can be defined as an event input.

Example diagram of input signals:

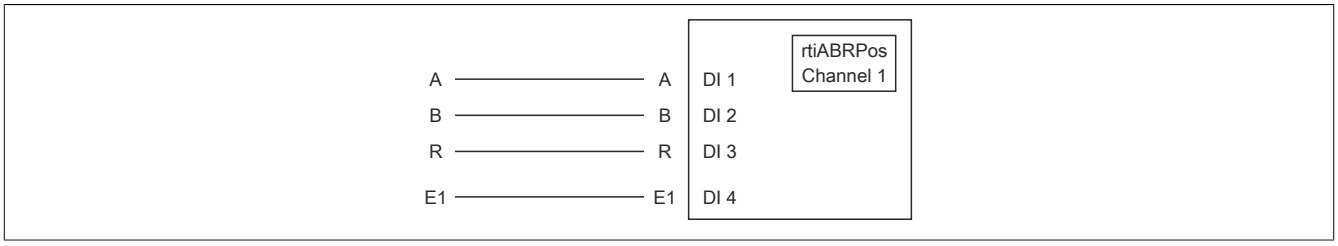


Figure 7: Schematic diagram of input signals for rtiABRPos

Using function block rtiABCnt

The following points must be taken into account when using function block rtiABCnt in a reACTION program:

- The function block can be used up to 3 times in a reACTION program.
- 2 digital inputs must be defined on the module for input signals A and B.
- In addition, up to 3 digital inputs on the module can be defined as event inputs E1, E2 and E3.

Example diagram of input signals:

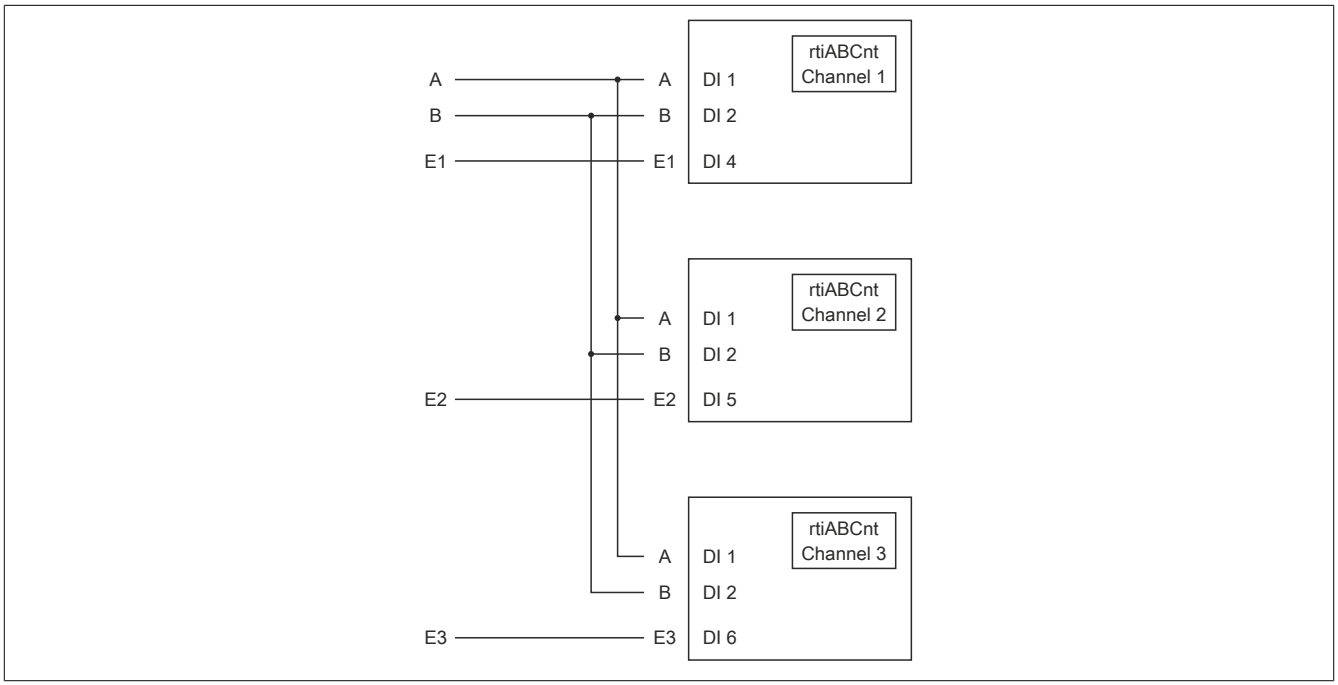


Figure 8: Schematic diagram of input signals for rtiABCnt

Using function blocks rtiABRPos and rtiABCnt in combination

The following points should be kept in mind when using function blocks rtiABRPos and rtiABCnt together in a reACTION program.

- Function block rtiABRPos can only be used once in a reACTION program.
- Function block rtiABCnt can be used up to 2 times in a reACTION program.
- 3 digital inputs must be defined for input signals A, B and R (rtiABRPos).
- The same digital inputs are used for input signals A and B (rtiABCnt).
- In addition, up to 3 event inputs E1, E2 and E3 can be defined (rtiABCnt).
- E1 is used for the event input (rtiABRPos).

Example diagram of input signals:

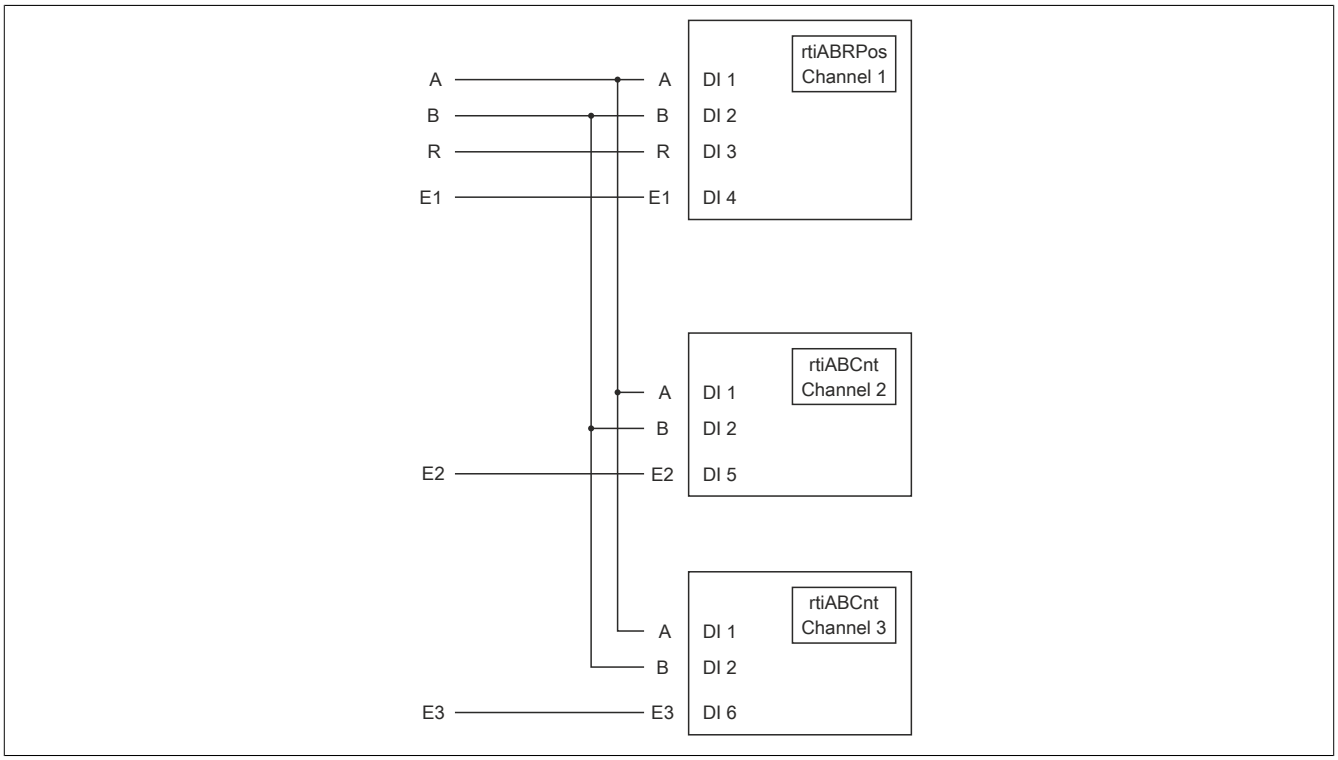


Figure 9: Diagram of input signals when using rtiABRPos and rtiABCnt at the same time

11.10.1.1 Registering the position encoder (rtiABRPos/rtiABCnt)

Name:
CfO_Config_ABR1

This register specifies the technical characteristics of the connected ABR incremental encoder.

Data type	Values
UDINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 15	Increments per revolution	0 to 65535	Reference pulse monitoring: If the reference pulse is different than defined here, this is indicated on the status output of function block rtiABRPos.
16	Inversion of the counting direction set by signals A and B	0	Positive counting direction
		1	Negative counting direction
17 - 31	Reserved	0	

11.10.1.2 Wiring the position encoder (rtiABRPos/rtiABCnt)

Name:
CfO_ChannelMapping1_ABR1
CfO_ChannelMapping2_ABR1

Before function blocks rtiABRPos/rtiABCnt can be processed by the reACTION engine, the hardware inputs to be used by the ABR incremental encoder must be defined on the module. The "ChannelMapping" registers specify which inputs are interpreted as the A, B, R, E1, E2 and E3 signals.

Data type	Values
UDINT	See the bit structure.

Bit structure of CfO_ChannelMapping1_ABR1:

Bit	Description	Value	Information
0 - 7	Input E1	0	Mapped to digital input 1
		1	Mapped to digital input 2
		...	...
		7	Mapped to digital input 8
		8 to 255	Reserved
8 - 15	Input R	0 to 255	For possible values, see bits 0 to 7.
16 - 23	Input B	0 to 255	For possible values, see bits 0 to 7.
24 - 31	Input A	0 to 255	For possible values, see bits 0 to 7.

Bit structure of CfO_ChannelMapping2_ABR1:

Bit	Description	Value	Information
0 - 15	Reserved	0	
16 - 23	Input E3	0	Mapped to digital input 1
		1	Mapped to digital input 2
		...	...
		7	Mapped to digital input 8
		8 to 255	Reserved
24 - 31	Input E2	0 to 255	For possible values, see bits 16 to 23.

Information:

For information about the relationship between the input on the module and the channel name, see section "reACTION function blocks - General".

11.10.1.3 Scaling the position encoder (rtiABRPos)

Name:
CfO_ScalingUnits_ABR1

CfO_ScalingIncrements_ABR1

An optional gear ratio can be configured using registers "Units" and "Increments". The dividend for scaling is defined in register "Units"; the divisor is defined in register "Increments".

Data type	Value	Information
UDINT	0 to 4,294,967,295	CfO_ScalingUnits_ABR1: Units per interval CfO_ScalingIncrements_ABR1: Increments per interval

Formula for calculation

Gear ratio = ScalingUnits / ScalingIncrements

Example 1

ScalingUnits = 1
ScalingIncrements = 1

Position value (Pos) = ABR increments * ScalingUnits / ScalingIncrements
Position value (Pos) = ABR increments * 1/1

In this example, the ABR position value is output unchanged on output "Pos".

Example 2

ScalingUnits = 10
ScalingIncrements = 4

Position value (Pos) = ABR increments * ScalingUnits / ScalingIncrements
Position value (Pos) = ABR increments * 10/4

In this example, the ABR position value is multiplied by 2.5 and output on output "Pos".

Information:

The encoder values are calculated internally as INT64 values in 32.32 format. On output "Pos" of function block "rtiABRPos", only the whole number value (INT32) is output for the user. The fixed point decimal places are used internally to calculate a higher resolution.

11.11 Direct I/O - Configuration

This module is equipped with 8 digital channels, 2 analog inputs and 1 analog output. In the "Direct I/O" function model, behavior is based on that of a standard module. The I/O channels are managed by an extremely simplified reACTION program. The function model primarily serves to check that the I/O channels are functioning properly.

11.11.1 Direction of digital channels

Name:
CfO_DigitalDirection

This register determines the signal direction of digital channels 3, 4, 7 and 8.

Data type	Values
UDINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	Direction - Digital channel 3	0	Input
		1	Output
3	Direction - Digital channel 4	0	Input
		1	Output
4 - 5	Reserved	0	
6	Direction - Digital channel 7	0	Input
		1	Output
7	Direction - Digital channel 8	0	Input
		1	Output

11.11.2 Filtering digital channels

Name:
CfO_DigitalFilter

This register defines the filter time of the digital channels. The filter value affects both the switching delay as well as the immunity of the channels.

Data type	Value
UDINT	0 to 500000: Units 10 ns

11.11.3 Filtering analog inputs

Name:
CfO_AnalogFilter01 to CfO_AnalogFilter02

This register sets the filter level of the analog input.

Data type	Values
UDINT	0 to 7

$$2^{AnalogFilter} = FilterLevel = \frac{Out(ADC)_t - Out(Filter)_{t-1}}{Out(Filter)_t - Out(Filter)_{t-1}} \cong \frac{\Delta Out(ADC)}{\Delta Out(Filter)}$$

The filter level results as the exponent to base 2 and corresponds to the ratio of the change of the digitalized input value to the change of the filtered analog value.

11.11.4 Limit values of the analog inputs

Name:
CfO_LowerLimit01 to CfO_LowerLimit02
CfO_UpperLimit01 to CfO_UpperLimit02

These registers define the upper and lower user-specific limit values for the analog input.

Data type	Values
DINT	LowerLimit: -32767 to 32767 (Default: -32767)
	UpperLimit: -32767 to 32767 (Default: 32767)

11.12 Direct I/O - Communication

This module is equipped with the following inputs and outputs:

- 4 digital inputs (sink) for 24 VDC
- 4 digital channels configurable as inputs (sink) or outputs (sink or source) for 24 VDC
- 2 analog inputs of type ±10 V
- 1 analog output of type ±10 V

11.12.1 Digital outputs

Name:
DigitalOutput03
DigitalOutput04
DigitalOutput07
DigitalOutput08

This register is used to predefine the value that should be output on the digital output.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	DigitalOutput03	0	FALSE
		1	TRUE
3	DigitalOutput04	0	FALSE
		1	TRUE
4 - 5	Reserved	0	
6	DigitalOutput07	0	FALSE
		1	TRUE
7	DigitalOutput08	0	FALSE
		1	TRUE

11.12.2 Digital inputs

Name:
DigitalInput01
DigitalInput02
DigitalInput03
DigitalInput04
DigitalInput05
DigitalInput06
DigitalInput07
DigitalInput08

This register indicates the value read for the respective digital input.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0	FALSE
		1	TRUE
1	DigitalInput02	0	FALSE
		1	TRUE
2	DigitalInput03	0	FALSE
		1	TRUE
3	DigitalInput04	0	FALSE
		1	TRUE
4	DigitalInput05	0	FALSE
		1	TRUE
5	DigitalInput06	0	FALSE
		1	TRUE
6	DigitalInput07	0	FALSE
		1	TRUE
7	DigitalInput08	0	FALSE
		1	TRUE

11.12.3 Analog inputs

Name:
AnalogInput01 to AnalogInput02

This register contains the analog input value.

Data type	Values
INT	-32767 to 32767

11.12.4 Analog output

Name:
AnalogOutput01

This register defines the value for the analog output.

Data type	Values
INT	-32767 to 32767

11.13 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

11.14 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs